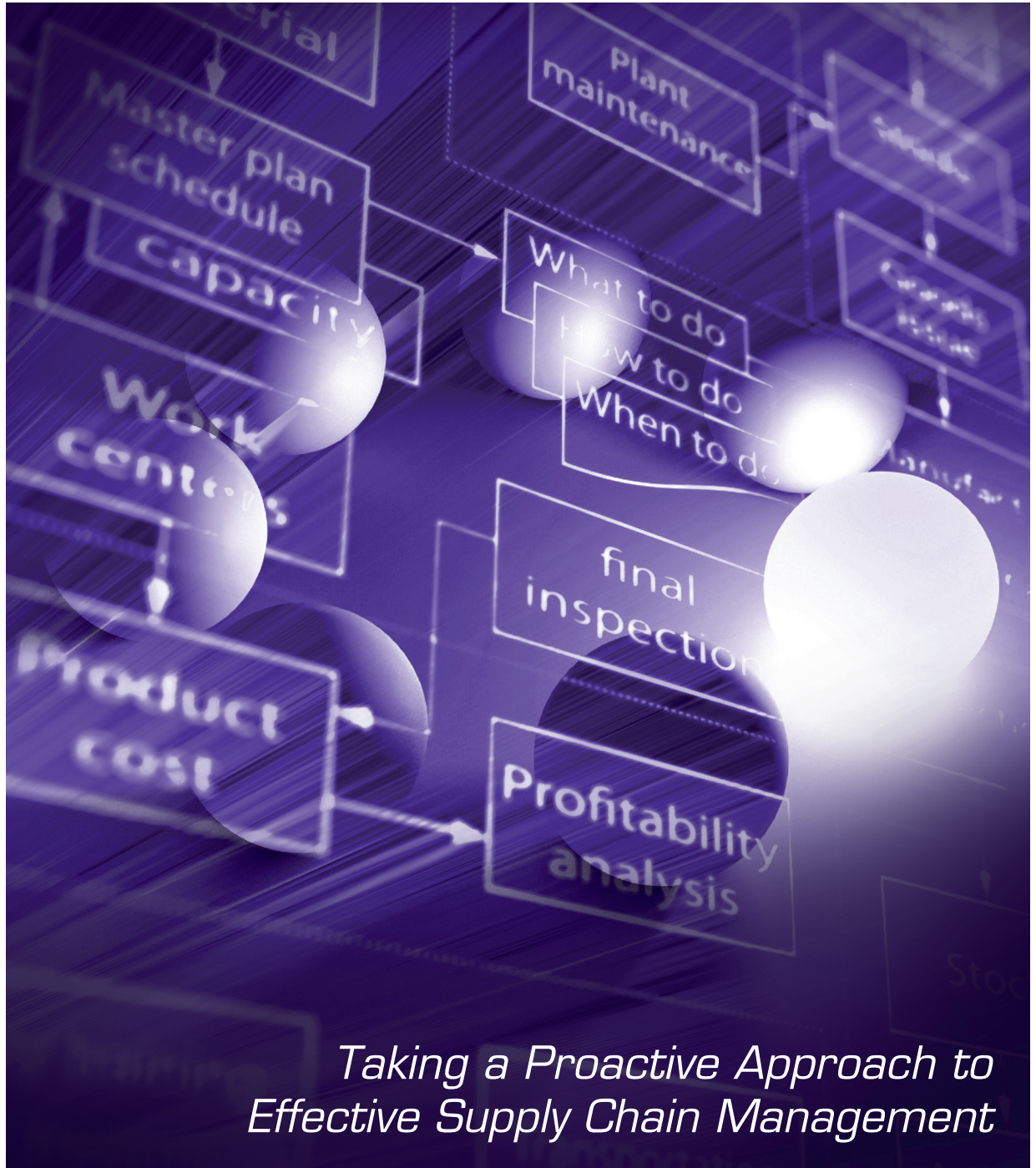*LEADERSHIP THROUGH GLOBAL COLLABORATION*

IS YOUR SUPPLY CHAIN READY FOR AN ECONOMIC RECOVERY?

HIDDEN LOGISTICS AND FULFILLMENT COSTS IN THE SEMICONDUCTOR SUPPLY CHAIN

WHAT'S YOUR RETURN ON DEVELOPMENT? IDENTIFYING THE KEY LEVERS AND MOVING THE NEEDLE

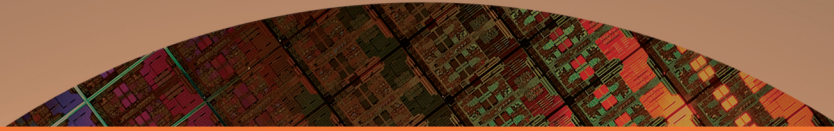*INTERNATIONAL CHALLENGES IN ENVIRONMENTAL COMPLIANCE AND SUPPLY CHAIN SUSTAINABILITY*

Taking a Proactive Approach to Effective Supply Chain Management

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from your Global Customers and Partners

CONTENTS

MISSION AND VISION STATEMENT

ACCELERATE THE GROWTH AND INCREASE THE RETURN ON INVESTED CAPITAL OF THE GLOBAL SEMICONDUCTOR INDUSTRY BY FOSTERING A MORE EFFECTIVE FABLESS ECOSYSTEM THROUGH COLLABORATION, INTEGRATION AND INNOVATION.

- Address the challenges and enable industry-wide solutions within the supply chain, including intellectual property (IP), electronic design automation (EDA)/design, wafer manufacturing, test and packaging

- Provide a platform for meaningful global collaboration

- Identify and articulate market opportunities

- Encourage and support entrepreneurship

- Provide members with comprehensive and unique market intelligence

Leadership through Global Collaboration

Kerry Enright, President, Enright Enterprise Consulting Solutions LLC

T he semiconductor industry leads the world in innovation, leveraging global partnerships as one of its keys to success. Yet is the industry really living up to its potential? To surmount current economic difficulties, the industry struggles to regain its momentum in leadership solutions through its various partnerships, but often these results fall short. The real problem, it appears, is that the industry focuses on partnerships but not true collaboration. What is the difference?

Working my way through college, I earned money by partnering on construction projects. In the first project, my partner and I started a block wall from different ends and worked towards each other. Upon meeting in the middle, we discovered that we had created a disaster. We changed our approach so that we always started at the same end, alternating mortaring and setting the block along our mutual guideline. As the wall rose, we arranged our staging to enable us to remain face to face and task to task through completion. This typified the essence of collaboration.

Our collaboration succeeded on the following elements:

- Standardized material of exchange.
- A mutual guideline.
- A common, real-time and interactive process.

How can semiconductor executives create such collaboration on a global basis, when in their own buildings their engineers on the first floor do not share processes with their engineers on the second? Since programs falter on the basics, how can collaborators deliver the right process to the right people at the right time?

The Shortcomings of Partnerships

Partnerships are plentiful in the semiconductor industry, but these partnerships struggle with execution challenges.

Standardized Material of Exchange

The most basic material of exchange, the document, can create execution barriers. There was a case where the engineer of a foreign partner sent the U.S. partner a design document that the U.S. partner believed to be approved. Based on this, they commenced their development. When the foreign partner's executives later denied that the design document was approved or supported, the U.S. partner backtracked on their development, losing months of development. Document exchange with multiple partners through team rooms creates similar vulnerabilities.

Partnerships seldom standardize their medium of exchange by defining the following:

- The document state: draft, preliminary, approved and released.
- The document version: V1.0 – Vn.n.
- The document status: in development, idle, in approval and in rework.
- The document location: physical and logical.

Without these basics, partners struggle as if they are working on opposite sides of a high wall.

Similarly, data is a fundamental material of exchange. While some partners succeed in creating common data dictionaries using naming conventions and formats, the challenges do not end there. Equally important, partners must facilitate data access. Eliminating "data rummaging" requires systems to capture, store and transfer fab process data to the right users based on who owns what data, what data is to be shared and what remains proprietary.

A Mutual Guideline

In construction, a taut guideline aligns processes to produce correct results. The same applies to the semiconductor industry, but the guideline contents are more complex—ground rules, specifications, intellectual property (IP) and assets.

Partnerships often fail to create common guidelines that produce the right results. How often do partners fail to agree on whether to use industry-standard design ground rules versus their own proprietary rules, when even something as simple as standardizing built-in self-test (BIST) greatly enhances a design? Guidelines on which design tool to use are likewise critical since different tools can produce different results to the same design problem.

Controlling specifications is a multi-headed task of creation, management and use. All specifications must reflect end-client needs, and since partners have different client views, they must create a coherent client advocacy within a joint management structure. This structure must compile and codify specifications before design start. Finally, a mutual guideline must decompose, disseminate and insert the specifications into each branch and level of design.

As with specifications, IP requires acquisition with the end client in mind. Since IP acquisition requires very extensive lead times, it must be planned far in advance. Individual companies typically field more requests for IP than they can afford, so partners working in conjunction need to coordinate their IP strategic plans if IP is to arrive just in time. Likewise, partners must support IP providers with standardized and common business engagement processes.

Partnerships imply sharing; and the more the partners share, the more critical becomes the relationship. But whenever sharing is involved, issues of value arise. Consider this. When multiple

companies come together, they naturally attach a value to the assets they bring to the common table. How then do the partners assess the value of what they and their partners offer so that all parties believe they received an equitable deal? This question escalates as the number of participants goes up. It also arises with IP acquisitions where the perceived value varies among the partners.

A Common, Real-Time and Interactive Process

Global partnerships exist to deliver converged products at a quality and cost attractive to clients. Unfortunately, many programs fail at the very beginning because of shortcomings in execution. Of these shortcomings, two stand out—client and manufacturing engagement.

The semiconductor industry resonates to extremely time-sensitive client demands, and new projects often start under severe schedule pressures. Frequently, this schedule pressure influences many partnerships to short cut the initial and most critical part of the program—concept and requirements definition. A poorly defined project concept or client requirements ripple down the design process and often result in project churn or design re-spins. Missed client requirements result in failed products.

Similarly, partner teams may lack assurance at program initiation that the designs are actually manufacturable across their disparate facilities. An obvious resolution to this problem engages manufacturing teams at the very outset of the program, but this approach proves cumbersome across multiple companies and is often omitted from program definition.

Once programs are underway, clear, formal reviews and handoffs between stages become paramount to ensure end-to-end linkage. Unless, however, the partners standardized their program linkages before the start, there is a high probability that broken couplings will plague their efforts.

The cash cow of the semiconductor industry thrives upon technology reuse—extending last-generation technology into incremental marketplaces. The secret to reuse is the creation of viable variants out of a common technology. Common technology, in turn, arises from disciplined design and manufacturing processes. Many semiconductor companies find maintaining a common technology challenging even for in-house needs, but when the opportunities extend over multiple companies, the task becomes exponentially more difficult.

Finally, companies evolve and even partners' strong initial commonality efforts face the prospect of divergence over time. Any attempt at cooperation, therefore, must also include plans for continuation.

Opportunities for Collaboration

If global collaboration requires standardized material of exchange, a mutual guideline and a common, real-time and interactive process, how can semiconductor executives create capabilities out of their disparate environments? The following highlights a method.

Process Management – Standardized Material of Exchange

Collaboration provides opportunities for standardizing materials of exchange. Since most companies have entrenched methodologies inherently resistant to change, introducing a collaborative environment opens the door to new methods—a superset of the individual companies. Operational executives can leverage their joint relationship to win greater degrees of freedom in standardizing common process exchange.

Process Standardization

Step one is to create simplicity in the face of complexity. Standardization of building materials enabled the efficient construction of homes and offices from worldwide product sources. The same principle applies to collaborative business processes.

Companies can standardize processes in the following manner:

- Radically reduce process logic into the simplest model that always delivers complete, correct and timely execution.
- Create a building block out of that model by embedding standard management functions.
- Tailor building blocks to specific tasks using pre-defined best-of-breed process templates.
- Construct maxi-enterprise execution logic out of the building blocks.

Figure 1. Process Management Method
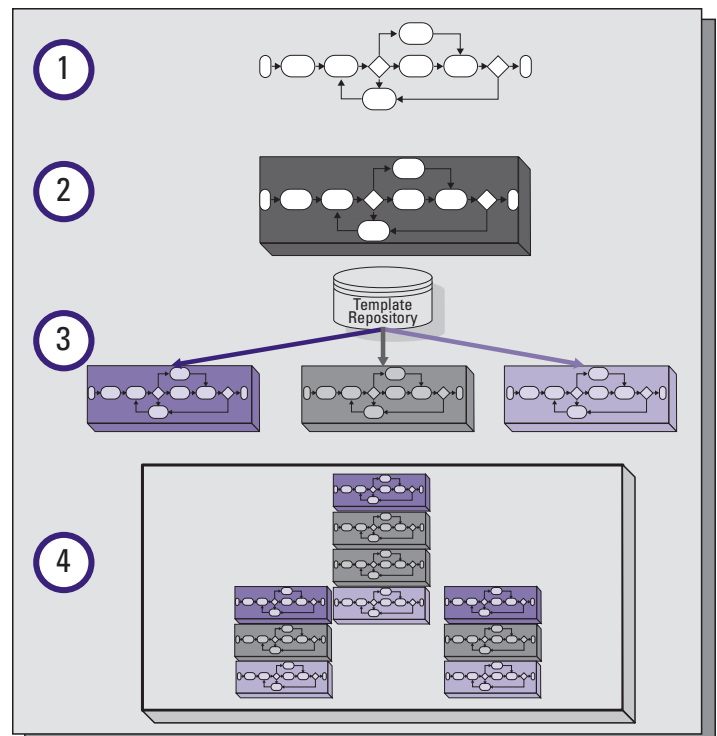
Note that the Figure 1 structure is not an application but an engine. Applications wait for instructions that derive from the enterprise execution logic. Engines embody enterprise execution logic and summon applications for procedures and functions that fulfill the logic.

Process Universals

All processes require a basic suite of functions to achieve complete, correct and timely execution. These functions manage state, version, status and location of any document, program or program sub-component. Additionally, performance monitoring provides essential support for process control and continuous improvement. By packaging such elements within process models, alliance participants can create execution hubs.

Execution Hubs – Mutual Guidelines

Execution hubs create mutual guidelines for classes of users. Every cooperative enterprise is nothing if not a collection of interested

Actel's (NASDAQ: ACTL) radiation-tolerant RTAX digital signal processor (DSP) field-programmable gate arrays (FPGAs) have completed qualification in accordance with the military and aerospace industry standard MIL-STD-883 Class B specification. This qualification expands Actel's support of high-speed signal processing applications for space payloads and exemplifies its ongoing innovation and commitment to serve designers of spaceflight systems.

Advanced Analogic Technologies (NASDAQ: AATI) introduced the AAT282X active matrix thin-film transistor (TFT) liquid crystal display (LCD) direct current/direct current (DC/DC) converter family which includes a white light-emitting diode (WLED) driver and VCOM buffer to enable the delivery of a fully integrated power solution for portable backlit displays. Key target applications include automotive displays, digital photo frames, netbooks, e-readers and handheld global positioning system (GPS) navigation devices.

Altera (NASDAQ: ALTR) enhanced its Arria II GX FPGA variant with 6.375 Gbps transceivers and up to 1.25 Gbps low-voltage differential signaling (LVDS) support, while broadening the reach of the family with the addition of the new Arria II GZ FPGA variant. As a result, the 40 nm Arria II family provides the lowest power 6 Gbps transceiver solutions shipping today, featuring up to 50 percent lower static power over competitive devices.

The newest member of the **Broadcom** (NASDAQ: BRCM) Intensi-fi product family revolutionizes how users can experience multimedia content in their homes. The BCM4331 Wi-Fi solution achieves 450 Mbps data rates in client devices and over 600 Mbps throughput (Transmission Control Protocol/Internet Protocol (TCP/IP)) in 3x3 access point (AP)/router configurations.

Skelmir has ported their CEE-J virtual machine (VM) to **Cavium Networks'** (NASDAQ: CAVM) ECONA CNS3XXX processors for the support of Open Services Gateway Initiative (OSGi) and other Java applications. The ECONA CNS3XXX family of ARM-based energy-efficient processors offers single and dual ARM11 MPCore processors, a rich set of integrated hardware accelerators and a range of inputs/outputs (I/Os) for glue-less voice, video and data connectivity.

CHiL Semiconductor announced a breakthrough in high-efficiency computing voltage regulator (VR) solutions for central processing unit (CPU), graphics processing unit (GPU) and double data rate (DDR) applications. Now configured to optimize efficiency from the lowest idle state to the highest operating state of today's high-performance server, graphics and desktop solutions, CHiL's next-generation true-digital power algorithms have increased efficiency up to 15 percent, especially at low loads.

Cortina Systems introduced CS4340, the industry's smallest quad 10 GB electronic dispersion compensation (EDC) device. The Cortina CS4340 is a programmable four-port small form-factor pluggable physical layer (SFP + PHY) with integrated EDC and is available in a small 15 mm x 15 mm ball grid array (BGA) package that optimizes system design options.

Fujitsu Limited selected **Cypress Semiconductor's** (NASDAQ: CY) TrueTouch solution to implement the touchscreen in the world's first separable handset from NTT DOCOMO, the DOCOMO PRIME series F-04B mobile phone. The new phone leverages Cypress' CY8CTMG200 controller to power the robust multi-touch interface with a slim 9.8 mm form factor that can operate separately from the keyboard.

Dialog Semiconductor (FWB: DLG) signed a licensing agreement to use NXP's ultra low-power embedded digital audio signal processor technology, CoolFlux DSP, and accompanying firmware, including NXP Software's LifeVibes voice speech enhancement engine. The move by Dialog is the next step in a strategic initiative to develop and deliver market-leading standalone and integrated power management and audio ICs with highly differentiated feature sets. Integration of the NXP DSP allows multiple audio decoding algorithms to be supported, including the facilitation of advanced speech processing algorithms.

Discera announced the official opening of its China Applications Center in the Shenzhen International Chamber of Commerce Tower on Fuhua 3rd Road, Futian District. As the heart of the company's permanent investment plan in China, the new office features engineers, equipment and researchers to support sophisticated chip and module integration, high-definition (HD) and 3-D video technology, and radio frequency (RF) and smart grid design.

To enhance the growth of the universal docking station market, ASUS has chosen to integrate **DisplayLink's** Universal Serial Bus (USB) virtual graphics processor, the DL-165, into the ASUS USB universal docking station.

Exar (NASDAQ: EXAR) introduced the DX 1700 series of Peripheral Component Interconnect (PCI) Express-based cards for the emerging unified storage and network infrastructure. The DX 1700 series is comprised of four cards and offers customers the industry's most power-efficient encryption and compression solutions addressing the small office/home office (SOHO) to enterprise markets.

Fresco Microchip was recently recognized as the fastest growing fabless semiconductor company in the industry. In June, Fresco announced that it has ramped from initial production to more than 15 million chips for the hybrid television market in less than three quarters. Eight of the top 10 TV tuner manufacturers are now in production or have active designs using Fresco inside, including LG Innotek, Panasonic Electronic Devices, NuTune and most recently Sanyo Tuner. According to industry experts, the company will be a top supplier of hybrid television receivers in Europe this year.

Gennum (TSX: GND) announced that its serial digital interface (SDI) solutions have been selected by Panasonic for use in industry-leading professional quality 3-D video equipment. With 3-D TV growth outpacing that of HDTV, demand for 3-D programming and content is on the rise.

NETGEAR selected **Gigle Networks'** GGL301 HomePlug AV/Institute of Electrical and Electronics Engineers (IEEE) 1901 solution with Xtendnet intelligent switching technology to give its XAV101V2 powerline adapters best-in-class network coverage and reliability in the home.

GigOptix (OTCBB: GGOX) made additional shipments of its LX8900, a 100 GB thin-film polymer-on-silicon (TFPS) modulator, to a number of customers including SA Photonics, an engineering company focused on photonics-based solutions for military applications.

Icera announced that its Livanto chipset and adaptive wireless technology is at the heart of Vodafone's latest mobile broadband USB stick, the Vodafone K3805-Z. Offering a high-speed mobile broadband connection with theoretical peak downlink rates of up to 14.4 Mbps High-Speed Packet Access (HSPA) in optimal conditions, the Vodafone K3805-Z is the world's first USB modem to incorporate Icera's IceClear interference-aware technology.

Digital China Holdings Limited will distribute **Impinj's** Speedway family of radio frequency identification (RFID) reader and antenna products throughout China. The new relationship ensures that Chinese RFID solution providers now have easy access to the world's leading ultra-high frequency (UHF) Gen 2 technology for a wide variety of applications and markets.

Infineon Technologies AG (FSE: IFX) introduced an enhanced family of three wireless control receivers offering the highest available sensitivity and low-power consumption. The TDA5240, TDA5235 and TDA5225 devices provide multi-band support for worldwide coverage and are well-suited for use in various automotive applications,

including remote keyless entry (RKE) systems, tire pressure monitoring systems (TPMS), remote start, control, status and alarm functions.

Innovasic Semiconductor unveiled its new RapID Platform connectivity solution for EtherNet/IP adapters. Innovasic's RapID Platform provides quick and easy EtherNet/IP connectivity, and engineers can download the entire platform free of charge for evaluation. A one-time license fee applies only if the platform is used in production.

International Rectifier (NYSE: IRF) introduced a family of hexagonal field-effect transistor (HEXFET) power metal-oxide semiconductor field-effect transistors (MOSFETs) featuring ultra-low on-state resistance (RDS(on)) in an industry-standard small-outline transistor (SOT)-23 package for applications including battery charge and discharge switches, system and load switches, light load motor drives and telecom equipment. Utilizing IR's latest mid-voltage silicon technology, the new SOT-23 MOSFET devices deliver a strong improvement in current handling by minimizing Rds(on) by as much as 90 percent to offer customers optimized performance and price for a given application.

AdaptivEnergy partnered with **Jennic** to offer alternative energy solutions for active RFID tag applications that can offset associated costs and risks inherent with battery-powered devices. Jennic's asset tracking platform uses IEEE802.15.4 technology to provide a robust active RFID solution with low-power requirements, allowing for tags with extended battery life or tags powered solely by harvested energy.

LSI (NYSE: LSI) and Seagate announced the delivery of a complex integrated read channel technology for Seagate's latest hard disk drive (HDD) products. Together, the companies have enabled the industry's first HDDs with low-density parity check (LDPC) read channel in 65 nm process system-on-chip (SoC) technology.

MediaTek (TSE: 2454) joined the Open Handset Alliance. Sharing the same commitment and vision for richer mobile living, the Open Handset Alliance is a partnership of more than 71 global mobile industry leaders aimed to accelerate innovation and offer consumers a richer and connected mobile experience.

Mellanox Technologies' (NASDAQ: MLNX) ConnectX-2 InfiniBand adapters and IS5000 InfiniBand switches have demonstrated world-record Message Passing Interface (MPI) performance for node-to-node communications. Recent cluster benchmarking performed at Mellanox's performance optimizations lab highlights Mellanox InfiniBand's achievement of nearly 90 million messages per second for MPI message rate for node-to-node communications, more than three times better than other comparable InfiniBand solutions.

Microsemi (NASDAQ: MSCC) unveiled a compact, cost-effective four-port power-over-Ethernet (PoE) midspan designed to power a wide range of network devices in low-density applications. Microsemi's new PowerDsine PD-3504G midspan is fully compliant with IEEE 802.3af specifications to safely power wireless local area network (WLAN) APs, IP security

cameras, voice over IP phones, access control systems and other devices over existing standard Ethernet cabling.

Nanoradio launched NRX600/605, the Eco-Fi family of products. Nanoradio is now able to significantly strengthen its customers' products and further enrich the user experiences of embedded consumer electronics powered by the new solution. The product family, which is supporting 802.11 b/g/n standards, gives outstanding power and area savings, unwiring new economically and ecologically innovative customer products.

Nordic Semiconductor ASA (OSE: NOD) released nRFready R/C Racing, a complete reference design for advanced remote controlled racing toys that enables toy manufacturers to bring previously impossible game-play features to mass-market toys by using Nordic's low-cost 2.4 GHz wireless solutions.

Octasic announced the industry's most efficient multi-core DSP device for basestation PHY and Media Access Control (MAC), the OCT2224W. Delivering three times more power efficiency than any other DSP on the market today, the OCT2224W device provides the best performance-to-power ratio in the industry.

ParkerVision (NASDAQ: PRKR) entered into an agreement with its confidential baseband partner to supply RF chipsets that incorporate ParkerVision's d2p technology. The chipsets will be used with baseband processors sold to a leading mobile handset original equipment manufacturer (OEM) who is a significant customer of ParkerVision's baseband partner.

PMC-Sierra (NASDAQ: PMCS) announced the SRCv family of 6 Gbps Serial Attached Small Computer System Interface (SCSI) Redundant Array of Independent Disks (RAID)-on-chip (RoC) controllers, including the industry's first 24-port RoC, which enables the highest levels of server performance and connectivity, along with an eight-port RoC targeted at the volume x86 server market.

Qualcomm (NASDAQ: QCOM) and Medical Platform Asia signed a formal agreement to provide medical devices with integrated 3G wireless modules for people in need of health services. The project is being implemented through Qualcomm's Wireless Reach initiative and will allow 300 remote local residents to send critical health information to doctors through a 3G wireless network. Information such as a resident's blood pressure, weight and distance walked can be easily and immediately shared with participating physicians.

RF Micro Devices (NASDAQ: RFMD) announced the RF5616, a highly integrated 4.9 GHz to 5.8 GHz (industrial, scientific and medical (ISM) band) 3 mm x 3 mm power amplifier designed to significantly reduce customers' total solution size and cost. The RF5616 is targeted for high-performance mobile PC and embedded applications including APs, gateways, digital subscriber line (DSL) routers, Wireless High-Definition Interface (WHDI) and WLAN for wireless video distribution networks.

Sigma Designs (NASDAQ: SIGM)

announced the first low-cost Microsoft Mediaroom-compatible set-top box (STB) platform based on Sigma's SMP8652 media processor SoC. SMP8652-based STB designs have completed integration with Mediaroom client software and are anticipated to begin deployment with leading carriers in 2H 2010.

Samsung Electronics is leveraging one of **Skyworks Solutions'** (NASDAQ: SWKS) power amplifier modules for the GT-B3710, a high-speed 4G USB modem that is the world's first Long-Term Evolution (LTE)-commercialized device. Small and efficient, the SKY77706 LTE power amplifier (PA) module is designed for multiple handset and data card applications, and allows consumers to enjoy the benefits of high-speed data services such as advanced Web TV broadcasting, online gaming and Web conferencing.

Toshiba America Electronic Components (TSE: 6502) and its parent company Toshiba launched a 128 GB embedded NAND Flash memory module, the highest capacity yet achieved in the industry. The module is fully compliant with the latest embedded-MultiMediaCard (e-MMC) standard, and is designed for application in a wide range of digital consumer products, including smartphones, tablet PCs and digital video cameras.

Ubicom introduced its IP8100 family of network processors. The processors are targeted towards next-generation solutions for consumer, SOHO and small/medium business (SMB) applications for both retail and service provider deployments.

VIA Technologies (TSE: 2388) released device development kits for the VIA AMOS-5000 series, facilitating a more rational design infrastructure for a broad range of application-specific and fan-less Em-ITX-based devices. VIA AMOS-5000 series development kits combine application-specific VIA EM-I/O expansion modules with specially designed extendable aluminum chassis kits.

WiSpry is working with IBM to develop micro-electromechanical systems (MEMS) process technology and manufacture its tunable RF product roadmap. This development includes WiSpry's current generation of tunable impedance matching products, slated for production with a major Tier-1 OEM this fall, as well as future generations of highly integrated products for the entire mobile terminal front-end.

Xelerated sampled its HX family of network processor units (NPUs), which are now available to system vendors and service providers. Based on Xelerated's unique and deterministic dataflow architecture, the HX family of NPUs can process 100 Gbitps of Ethernet traffic at wirespeed for any packet size.

ChipSiP Technology and **Zoran** (NASDAQ: ZRAN) collaborated to produce a new slim package solution for the compact digital camera market that includes both multi-memory and an image processor. This new packaging solution helps designers save space on digital camera design boards and shorten the interconnection distance between electric components, significantly improving performance. ∎

Is Your Supply Chain Ready for an Economic Recovery?

Jim Takach, Director, PRTM

Companies across many industries believe that the worst of the downturn has come to an end. After making massive cutbacks over the past couple of years, they are starting to see an increase in demand. This development is good for semiconductor companies, but it also presents some significant challenges.

According to PRTM's recent global survey[1], companies across many sectors, on average, expect their revenues to grow more than 8 percent annually through 2012. More than one third of the companies surveyed expect average gross margins to exceed 20 percent by 2012; two thirds expect gross margins to surpass 10 percent. While the responses vary by industry, the numbers as a whole stand in strong contrast to just a year ago, when many companies experienced flat or declining sales and struggled to produce profits.

But are supply chains ready for the upturn? Many executives doubt their companies have the capabilities needed to meet rising demand and the greater complexity it will impose on the supply chain.

The findings of this year's survey throw light on the concerns that companies are experiencing as they prepare for the economic recovery. A significant number of the survey's nearly 350 respondents were original equipment manufacturers (OEMs) and suppliers from major sectors served by semiconductor companies, including the electronics, communications, industrial equipment, medical device, automotive, and aerospace and defense industries. Given the end-to-end nature of today's supply chains, the challenges that customers face are as important for semiconductor companies to understand as the ones they face themselves.

Key Survey Findings

This year's survey revealed five key themes:

Supply Chain Volatility and Uncertainty Are Here to Stay

Nearly 75 percent of all survey respondents consider demand volatility and poor forecast accuracy the greatest supply chain challenge. Additionally, nearly 25 percent said supplier quality and on-time delivery were major concerns.

During the recession, customer buying patterns changed dramatically and became even more difficult to predict. As companies slashed prices and end customers focused more on value, demand volatility grew, making accurate forecasting increasingly difficult. This behavior will likely continue. And even in cases where demand improves, the capacity cutbacks that suppliers enacted to weather the downturn have made it difficult to ramp-up production.

To address these challenges, semiconductor companies need to ensure they have visibility as far "downstream" in the supply chain as possible. Both they and their customers must strengthen capabilities to effectively plan and respond to changes in demand. This requires solid management processes, strong organizational capabilities, and the right systems and tools.

Securing Growth Requires Global Customer and Supplier Networks

The survey suggests that global expansion and customized products will be key sources of future growth. More than three fourths of respondents anticipate an increase in the number of international customer locations, and more than two thirds expect an increase in the number of products or product variants to address future market needs. And, notably, more than 85 percent expect the complexity of their supply chains to increase significantly by 2012.

To overcome these hurdles, companies must make sure that their global supply chain networks are designed to cost effectively serve the evolving market base, and that their supply chain organizations have the capabilities needed to manage these networks. This requires staying close to customers and to their customers' customers—critical for keeping up with changing supply chain footprints.

Figure 1. Drivers of Supply Chain Complexity

Percentage of participating companies expecting an increase (multiple answers possible)

Increase in customers or customer locations	79%
Increase in products/variances offered	67%
High fluctuations in customer orders	65%
Increase in strategic suppliers	51%
Increase in manufacturing facilities	47%
Increase in distribution facilities/inventory locations	44%
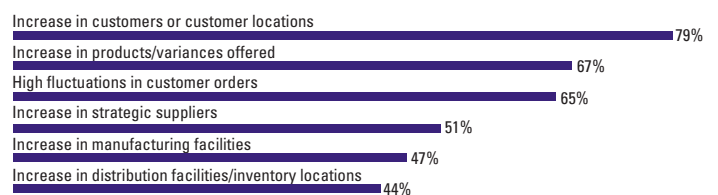
Market Dynamics Demand Regional and Cost-optimized Supply Chains

Outsourcing is on the rise as companies try to cut supply chain costs and increase flexibility. When asked what they keep in-house versus what they outsource, companies surveyed said they outsource 40 percent of their warehousing and transportation, about 30 percent of their manufacturing and nearly 25 percent of their final assembly. Although outsourcing has provided significant labor and material savings, many companies did not report reductions in process or management costs.

Outsourcing is an effective strategy for reducing operating costs, but additional overhead may be required to manage these operations. Companies need to get a better handle on the management and process costs that can fly under the radar. Total supply chain cost engineering is a useful tool in this regard.

Companies Must Take a Broader Approach to Supply Chain Risk Management

The survey results indicate that managing risk across the entire supply chain—from demand planning to expansion of manufacturing capacity—is an imperative. Respondents noted that effective risk management requires a multifaceted strategy. Nearly 70 percent said that additional risk mitigation strategies, such as steps to improve inventory management and delivery performance, were at the top of their agenda. These focus areas are part of a much broader approach to supply chain risk management, as customer companies shift more risks upstream to their suppliers.

This approach marks an important departure from the recent past. During the global financial crisis, many companies concentrated their efforts on minimizing the risk of supplier defaults and other issues with the potential to disrupt supply quality and delivery. While this is still a priority, it does not rank as highly as other risk mitigation strategies.

In view of these findings, supply chain executives must take an end-to-end view of risk management—from demand planning to the extended supply chain footprint. They should include not only the internal supply chain organization, but also supply chain partners—OEMs and suppliers—when forming supply chain risk management strategies. This is vital for companies throughout the value chain.

Figure 2. Top Strategies to Reduce Risk and the Negative Impact of the Downturn

% of participants that pay significant attention to the following risk mitigation strategies by 2012

Strategy	%
Effective inventory/stock management	69%
Improve delivery performance to customers	69%
Focus on profitability and cash management	68%
Service innovation and product lifetime management	64%
Reduce order fulfillment lead time	63%
Simplification of the global supply chain footprint	61%
Reduce your company's carbon footprint	60%
Accelerate new product introduction	59%
Extend your global supply chain footprint	55%
Tightly manage supplier risk	54%
Optimize accounts payable and receivables management	49%
Improve product quality/safety	45%

Existing Supply Chain Organizations Are Not Equipped for the Challenges Ahead

Problems with the supply chain organization stand in the way of many companies wishing to capture the benefits of the recovering economy. Nearly 30 percent of respondents indicated their supply chain organizations lack the integration and collaboration needed to ensure that decisions are optimal for all supply chain functions. And nearly 25 percent indicated their organizations are unable to make decisions quickly in response to sudden changes in demand.

Leading companies across industries understand that breakthrough improvements mandate the integration of key functions, such as product development and manufacturing, and their close collaboration in areas such as new product introductions and ongoing lifecycle management. These companies also make sure to empower their supply chain managers so they can facilitate

optimal decisions and execute end-to-end improvements.

Semiconductor companies would be well-served adopting these practices. In the future, corporate performance depends increasingly on a supply chain organization which effectively collaborates with other business units, and which maintains clearly defined roles and accountabilities, and strong talent.

Industry-Specific Findings

The findings for the automotive, electronics and communications, and industrial sectors—many of which rely heavily on semiconductor products and services—are also worth noting.

Automotive

Today's outlook for the automotive sector is rosier than recent years as automotive companies expect increasing customer demand for a generation of cars that provide higher fuel efficiency, in-car entertainment and other features. Survey participants from the automotive industry expect 9 percent annual revenue growth over the next three years and average gross margins to surpass 10 percent by 2012.

While demand volatility is a challenge for automotive, in some ways the sector is better prepared than others to address it. A high number of automotive respondents indicated they have streamlined product development and manufacturing processes and have adopted strong modularity standards and component standardization—all of which enable a flexible response to market changes.

Electronics and Communications

Companies in these sectors are optimistic about financial health: Nearly half expect gross margins of at least 20 percent by 2012. Optimism is greatest in companies based in Asia and Europe.

Nearly 90 percent of electronics and communications respondents indicate demand volatility and forecast accuracy to be a major challenge. Response strategies include cycle-time reduction, component and module standardization, joint planning with customers, better demand sensing, and improvements to warehousing and logistics.

The sector also sees continued cost pressures. To achieve the needed reductions, companies envision further outsourcing of manufacturing, warehousing and logistics, and after-sales service and repair.

Industrial

More than 80 percent of industrial respondents said demand volatility is a major concern. Not coincidentally, the survey also indicated that industrial companies' demand forecasting is in need of significant improvement. One third of respondents update forecasts with their key customers only once a quarter, and nearly half do so once a month. These companies would do well to follow the example of leading companies which update their forecasts more frequently.

Manufacturing flexibility is also a priority. More than 90 percent of manufacturing respondents plan to focus on cycle-time reduction, and nearly 80 percent are moving to a make-to-order strategy. These companies also highlighted continued focus on supplier lead times and capacities.

austriamicrosystems recently celebrated the 4th anniversary of high-volume production of its best-in-class 120 V 0.35 µm high-voltage CMOS process. Successfully introduced already in May 2006, foundry customers benefit from a fully qualified, high-volume production-proven and mature high-voltage CMOS technology ideally suited for emerging applications such as sensor interfaces, power-over-Ethernet (PoE), motor controllers and a variety of automotive applications.

The H35 specialty foundry technology allows the integration of 3.3 V, 5 V, 20 V, 50 V and 120 V n-type metal-oxide semiconductor (NMOS) and p-type metal-oxide semiconductor (PMOS) devices on a single chip without any process changes. H35 is the first purely CMOS-based high-voltage foundry process that matches bipolar/CMOS/DMOS (BCD) performance and chip sizes at much lower process complexity. Rigorous modularity permits 100 percent reuse of low-voltage CMOS design intellectual property (IP). Offering fully scalable high-voltage NMOS and PMOS devices, floating logic libraries as well as a best-in-class power-on resistance makes the 120 V high-voltage CMOS technology a compelling solution for fabless design houses and integrated device manufacturers (IDMs).

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Synopsys, a world leader in software and IP for semiconductor design, verification and manufacturing, and **GLOBALFOUNDRIES,** a leading provider of advanced semiconductor technology and manufacturing services, announced an agreement to develop the Synopsys DesignWare SuperSpeed Universal Serial Bus (USB) 3.0, USB 2.0, High-Definition Multimedia Interface (HDMI) 1.4 transmitter (Tx) and receiver (Rx), double data rate (DDR)3/2, Peripheral Component Interconnect (PCI) Express 2.0 and 1.1, Serial Advanced Technology Attachment (SATA) 1.5/3 Gbps and 6 Gbps, and Attachment Unit Interface (XAUI) physical layer (PHY) IP for GLOBALFOUNDRIES' 28 nm gate-first high-k metal gate (HKMG) process technologies. The collaboration will enable mutual customers to differentiate their 28 nm designs with a high-quality IP portfolio targeted at next-generation electronic system-on-chips (SoCs). The long-standing relationship between the two companies has resulted in the successful development of DesignWare PHY IP from 180 nm to 32 nm process technologies. GLOBALFOUNDRIES and Synopsys are the first to announce the development of USB, PCI Express, DDR,

HDMI, SATA and XAUI PHY IP targeting 28 nm process technologies with scalability to future generations.

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MagnaChip Semiconductor, an Asia-based designer and manufacturer of analog and mixed-signal semiconductor products, announced that it now offers an enhanced process design kit (PDK) for 0.18 µm and 0.35 µm BCD technology which has been receiving industry-wide attention. The latest PDK features major advancements from three key perspectives: user environment, PDK content and design support. More specifically, functions such as a one-click download, PDK installer and auto-version matching enable rapid automatic setup of PDK conditions, creating a user friendly environment. A layout utility is also provided to support global net connection, seal ring and guard ring.

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Samsung Foundry qualified the industry's first 32 nm high-k metal gate low-power (HKMG LP) process in May 2010, an optimized solution for customers' next-generation mobile and consumer products. Designers now can access this advanced leading-edge technology with proven IP and standard cell libraries in their development of advanced products. Volume production of 32 nm HKMG process products is scheduled for the beginning of 2011.

Samsung Electronics' foundry business is dedicated to supporting fabless companies and IDMs by offering full-service solutions, which encompass design kits and proven IP to full turnkey manufacturers, to achieve market success with advanced IC designs through foundry, application-specific IC (ASIC) and customer-owned tooling (COT) engagement. Samsung Foundry focuses on leading-edge process technology from 90 nm and below, and is currently in mass production at 45 nm and preparing next-generation 32 nm, 28 nm and beyond process technologies.

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Virage Logic, the semiconductor industry's trusted IP partner, and **Semiconductor Manufacturing International (SMIC),** the leading foundry in China, announced the

extension of their longstanding partnership in 40 nm low-leakage (LL) process technology. Building on the successful partnership that was initially established with 130 nm process technology, Virage Logic and SMIC have collaborated to provide mutual customers with highly differentiated IP for a broad range of SMIC's process technologies including 90 nm and 65 nm. Under the terms of the new agreement, SoC designers will have access to Virage Logic's SiWare memory compilers, SiWare logic libraries, SiPro Mobile Industry Processor Interface (MIPI) and Intelli DDR IP on SMIC's advanced 40 nm LL process. In addition, one key provision of this new agreement provides SMIC access to Virage Logic's advanced STAR memory system and STAR yield accelerator tools to accelerate the development, testing and yield enhancement of its 40 nm LL memory-related technology.

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SilTerra Malaysia is a proud winner of the Product Excellence Award 2009, which was given by the Ministry of International Trade and Industry (MITI) of Malaysia. This award recognizes SilTerra's leadership position and innovation in high-voltage technology for single-chip display driver ICs used in display panels of digital still cameras, feature phones and smartphones.

SilTerra has been continuously investing in research and development (R&D) activities to enhance its technology competitiveness. New technology such as 180 nm BCDMOS and 180 nm V-Tr MOS technology was introduced for customers to design-in for power management applications used in light-emitting diode (LED) drivers, motor drivers, direct current-direct current (DC-DC) converters, lithium battery chargers and more. These technologies are developed for energy-efficient power management applications, which is inline with global green initiatives.

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In June 2010, **Taiwan Semiconductor Manufacturing (TSMC)** reached an important milestone in the company's pledge to expand investment in Taiwan. This was achieved through the groundbreaking ceremony in Taichung's Central Taiwan Science Park for Fab 15, TSMC's third 12-inch (300 mm) Gigafab.

Fab 15 will be TSMC's third Gigafab, or fab with capacity of more than 100,000 12-inch wafers per month, and will also be TSMC's second Gigafab equipped for 28 nm technology. This will be TSMC's next "green fab" following Fab 12 and Fab 14, incorporating green concepts in energy conservation and pollution control in its design, including a process water conservation rate of 85 percent, reclamation of rainwater, recirculation and reuse of general exhaust heat, and development of solar power generation and LED lighting applications. TSMC's goal is to reach zero emissions of greenhouse gases.

TSMC is scheduled to begin equipment move-in for the Phase 1 facility in June 2011, with volume production of 40 nm and 28 nm technology products for customers in Q1 2012. Construction will be divided into four phases, and total investment over the next several years is expected to exceed NT$300 billion.

TSMC is the world's largest dedicated semiconductor foundry, providing the industry's leading process technology and the foundry's largest portfolio of process-proven libraries, IP, design tools and reference flows. The company's total managed capacity in 2009 exceeded 10 million 8-inch equivalent wafers, including capacity from two advanced 12-inch GigaFabs, four 8-inch fabs, one 6-inch fab, TSMC's wholly owned subsidiaries WaferTech and TSMC China, and its joint venture fab Systems on Silicon Manufacturing (SSMC). TSMC is the first foundry to provide 40 nm production capabilities. Its corporate headquarters are in Hsinchu, Taiwan.

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TowerJazz announced its 5th annual customer-focused technology conference—the TowerJazz Global Symposium (TGS)—to be held October 28, 2010 at its Newport Beach facility. TGS will focus on design enablement and will feature an industry outlook keynote from Gartner.

The company also announced its expanded business relationship with Vishay Siliconix to include increased production of its high-voltage power metal-oxide semiconductor field-effect transistors (MOSFETs) and super junction FET power MOSFETs.

TowerJazz was selected by Tego to manufacture its high-memory radio frequency identification (RFID) chips to be used by Airbus for improved aircraft maintenance and logistics. In addition, Canesta chose TowerJazz for its CMOS image sensor (CIS) technology to manufacture 3-D image sensors for consumer desktop computing, TV and entertainment applications.

TowerJazz also announced its further momentum in Korea with its global technology symposium and participation at the Institute of Electrical and Electronics Engineers (IEEE) International Memory Workshop to present its industry-leading non-volatile memory (NVM) technology.

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United Microelectronics (UMC) has partnered with Elpida and PTI to develop a fully integrated through-silicon via (TSV) solution suitable for a wide range of applications. Leveraging UMC's leading-edge logic technology and logic design interface with Elpida's dynamic random access memory (DRAM)/TSV technology and PTI's packaging and testing, this joint development project will allow UMC to provide foundry customers with a total solution for their 3-D IC designs that includes logic + DRAM interface design, TSV formation, wafer thinning, testing and chip stacking assembly. The resulting technology is expected to help fabless customers increase cost competitiveness, improve logic yield impact and accelerate entry into the 3-D IC market.

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X-FAB recently announced the industry's first 100 V high-voltage 0.35 μm pure-play foundry process. It enables a new class of reliable, high-performance battery monitoring and protection systems for battery management. It is also ideal for power management applications and for ultrasonic imaging and inkjet print head apps using piezoelectric drivers. In addition, X-FAB added new and enhanced N- and P-type double-diffused metal-oxide semiconductor (DMOS) transistors with 45 percent lower on-resistance for multiple operating voltages up to 100 V, lowering the silicon footprint by up to 40 percent and thus reducing die costs. Other device enhancements include Schottky diodes, 20 V and 100 V high-voltage capacitors, and bipolar transistors.

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Hidden Logistics and Fulfillment Costs in the Semiconductor Supply Chain

Marta Garcés, Vice President, Operations, ADD Semiconductor

Effective supply chain management enables companies to be more competitive in the world of manufacturing by reducing costs and improving customer service. The main purpose of a supply chain is, in fact, to make products available to customers in the right quantity, at the right time, with the best quality and in the most cost-effective manner.

When speaking about a semiconductor start-up's supply chain needs, the process becomes even more complex and critical as not only standard logistical problems and costs must be taken into account, but also storage, handling of the final product, and packaging quantities that may be limited by wafer size, thus making it a critical point to better manage the supply chain so as to handle possible quality problems reported by end customers. All these facts make it challenging for semiconductor start-ups and third-party logistics partners to implement strong, flexible supply chains.

The Everyday Problems of Global Sourcing

Today's modern semiconductor industry requires properly established and organized supply chains set up for maximum efficiency so as to avoid problems. The semiconductor market is truly global. Its major foundries primarily located in Asia and the United States ship sensitive materials all around the world using distributors that may not be familiar with the foundries' special characteristics such as specific security measures and tamper-proof locks. The market demand variability for these types of products is very high, generating different situations, from allocation problems to standard lead times and overstock management when demand falls abruptly, creating an uncertainty that makes logistics and supply chain planning a critical step.

A supply chain exhibiting no problems can still be in danger if suddenly faced with situations as simple as a storm or as critical as a political disruption or a strike. Therefore, even if a company outsources freight management to a third party, it must always know the status of what has been shipped or is due to be shipped at each stage of the supply chain. A lack of readily available information can also cause a company to not identify and solve problems in time.

If a supply chain is not correctly managed, a number of hidden effects may appear, all of which usually result in the company losing money and efficiency. Quality control throughout the chain is also of high importance, from material quality to the adequate packaging of goods and going through adequate and complete customs documents. The failure to meet any of these requirements can lead to a shipment delay or even damage the final product.

Another important point is the bureaucracy involved in shipping product. A misunderstanding of a country's custom rules and regulations can incur improper freight costs and inefficient deliveries. With overseas purchases being a daily routine in the semiconductor market, purchasing companies must work closely with their suppliers and make sure distributors have complete knowledge of all rules and regulations so as to avoid unexpected issues.

Also, bad planning, bad maintenance of safety stock inventory and last minute orders from customers due to lack of critical scheduling information at the fabless company can lead to very tight deadlines, delaying or changing shipments. This always involves the necessity of

using expedited transportation services which can double the cost of regular freights.

How a company manages its supply chain defines in some way its business, and therefore must continually study how to control and improve all aspects involved. A company's image can be seriously damaged by missed deadlines or late deliveries, putting them in a difficult position as they will have to explain to their customer how and why the system went wrong. That is why having all needed information readily available is crucial as it allows the chain to be informed about possible delays or problems.

Fabless-Specific Problems

Fabless start-ups must take into account not only standard logistics costs, but also costs that many times seem to be absorbed by the day-to-day work. These costs should be considered hidden logistic costs when analysis of margins and revenues is so critical in the early stages of company growth. The importance of knowing the real logistics costs is vital to obtaining the true financials of a company. It must be aware that these costs not only include those related to shipping.

The first barrier fabless companies encounter is the minimum order quantities (MOQ) companies must acquire even in ramp-up production. These quantities apply to those companies creating new business and having a small number of customers that are only testing new, possible suppliers and thus using small quantities of product. This requires a great effort in logistics such as a bigger warehouse to store incoming product, more days of inventory as it will take longer to sell product, and handling sensitive components during adequate installations with an ill-prepared staff.

This potential problem escalates when using special manufacturing processes. To maintain quality and traceability, each wafer manufactured is treated as a different lot, which means two realities must be taken into account:

- The number of chips on each wafer is not the same in every production as there is an indefinite number of wasted dies that does not remain the same from one production to another.

- To maintain product quality and traceability during the entire process, chips obtained from different wafers must not be packaged together in the same box so they can be uniquely identified and followed throughout the supply chain.

These issues also affect logistics in two ways:

- The number of packages received in each shipment and the quantity included is not known in advance and is difficult to control as it may vary from one production and/or delivery to the next. Therefore, expected delivery costs and warehouse placement can differ.

- It is difficult to transmit MOQs to final customers so as to reduce the internal handling of product, as the expected quantity in each box is not always the same and can't be known in advance.

Due to this matter, another and more critical problem arises—handling critical product. There is great risk involved if a fabless start-up receives an incorrect packaged quantity from its supplier, for example, and is therefore forced to open the original sealed package and manipulate product to make sure the correct quantity is shipped to its customer. The components could become damaged if the staff moving them does not possess the necessary skills and if they are moved under unfit conditions. There is also the difficulty of keeping the remaining product not shipped in a proper environment in terms of humidity, temperature and packaging. The company should invest in equipment such as vacuum packaging machines and small strapping machines, in material such as antistatic bags and extra trays, and in personnel dedicated to these tasks so the product is stored under the best conditions.

Obviously, these must be considered extra logistics and supply chain costs, not only taking into account delivery and warehouse costs, but also personnel costs. The company must be aware of these extra costs as they are many times hidden from those in charge of calculating the final product cost. Is it the responsibility of logistics and operations personnel to calculate the time and money invested in these everyday jobs so they can be added to the final cost of the product?

Some Possible Solutions

All these problems have to be seriously considered, as the supply chain can help emerging companies get introduced in new markets and is the most significant source of cost savings when all the previous issues mentioned are handled in the most efficient way.

Third-party logistics partners can assume some of the global sourcing issues that companies face such as warehousing and partnering with distributors. Direct relations with foundry, assembly and test subcontractors are also a necessity to have full visibility and traceability of product throughout the supply chain process and to respond to customer information requests in real time. These options, combined with adequate metrics, a good traceability system and new electronic tracking methods used by distributors to follow shipments in real time in each stage of delivery, give companies tools to control the supply chain. They also make it easier for companies to deal with future problems, solving them in the best way and in the shortest amount of time without affecting the end customer.

Problems inherent within start-ups are not easy to solve as only company growth can diminish them. It is a constant challenge for them to manage and reduce logistics costs. Efforts to reduce costs include, among others, negotiating directly with customers to adjust quantities to be delivered, minimizing the handling of material; planning supplier orders and shipments to be as adjusted to reduce inventory costs; and strengthening the structure of the company with the technical tools and personnel needed to face problems that must be managed once it is established and leaves its start-up condition.

The company must finally have the agility and ability to react promptly and appropriately to market conditions and have a strong, flexible supply chain. There are many tools and ways to achieve this. It is only a matter of choosing the correct ones and putting them to use within the company. ■

About the Author
Marta Garcés has a telecommunications engineering degree from the University of Zaragoza. Before joining ADD Semiconductor's staff, she worked for Siemens as corporate coordinator in the areas of quality, environment and European Foundation for Quality Management (EFQM), and in Kepar Electrónica firstly as R&D&i manager and later as project and international purchasing manager. At present, she performs the function of vice president of operations in ADD Semiconductor. You can reach Marta Garcés at marta.garces@addsemi. com or +34 690 014 749.

BackEND

Advantest introduced its scanning electron microscope (SEM)-based critical dimension (CD) measurement system for photomasks. Advantest's E3610 and E3620 CD-SEM advanced mask metrology tools enable photomask manufacturers to measure the critical dimension of the miniature-sized patterns in a photomask and assure accuracy in semiconductor manufacturing. These systems offer the precision and linewidth repeatability required to provide continuous yield improvement at the 65 nm and 45 nm production nodes, as well as support for 32 nm and 22 nm process development. The best-in-class E3610 and E3620 utilize Advantest's unique electron optical column design, enabling accurate CD control. They boast superior long-term operating stability and CD variation of less than ±1 nm, and are backed by the Advantest brand and the company's renowned worldwide support infrastructure.

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Amkor Technology and Texas Instruments (TI) announced they have qualified and begun production of the industry's first fine-pitch copper pillar flip-chip packages—shrinking bump pitch up to 300 percent compared to current solder bump flip-chip technology. Co-developed to lower the packaging costs of IC devices with fine-pitch input/output (I/O) pad structures of less than 50 μm, this proprietary technology platform also boosts performance, making it ideal for wireless and embedded processing applications based on plated copper pillar bumping and assembly technology.

Working together, Amkor and TI rapidly developed, qualified and deployed this new package platform that will not only address TI's flip-chip package needs

for the next decade but will also serve as a game changer for the industry. This new lead-free technology enables the use of flip-chip interconnection at fine pad pitches (50 μm and smaller) using fine-pitch copper pillar bumping and a newly developed assembly process which acts as the platform interconnect technology for integration with next-generation advanced silicon nodes. It also typically reduces substrate layer count as compared to standard area array flip-chip, yielding a low-cost package solution. The package was developed for very thin die, which, when combined with the low standoff height of the copper pillar bump itself, reduces package height.

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DA-Integrated is the semiconductor industry's first and leading provider of comprehensive IC development and supply engineering services. DA-Integrated features a full suite of tools and expertise of a fabless semiconductor company, offered as pure-play services, complementing customers' core capabilities.

Finding the right provider for production testing of low-volume and high-complexity ICs is always a challenge, especially when global capacity is constrained. DA-Integrated's test operations group has grown to meet this increased demand. The company provides competitively priced production capability targeted specifically at this market segment. Access to support from the company's design, test development and supply engineering experts enhances the service, making DA-Integrated the world leader for engineering sampling, pre-production, reliability testing and low to medium volume production.

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Evans Analytical Group's (EAG) release-to-production (RTP) team provides engineering service and support from early chip design to volume production in the areas of test program development and product engineering; test time rental on all major automatic test equipment (ATE) platforms; reliability and environmental qualification; electrostatic discharge (ESD) and latch-up testing; printed circuit board (PCB) layout and hardware design; failure analysis; focused ion beam (FIB) circuit edit and debug; electron microscopy (transmission electron microscopy (TEM), SEM, dual-beam FIB/SEM); and equipment calibration and repair services. Coupled with 30 years of experience in materials characterization and surface analysis, EAG offers the broadest range of solutions of any commercial lab network.

EAG offers its customers a highly customizable and flexible service model. The company believes that each customer's needs require the right combination of resources, and outsourcing cannot take a one-size-fits-all approach. Many of EAG's fabless customers rely heavily on EAG's integrated model to support their product flow from conception to volume production, requiring full engineering support across multiple disciplines and services. EAG's larger fabless and integrated device manufacturing (IDM) customers are utilizing this model to support specific projects as a compliment

to their own resources. With the breadth of engineering expertise and services and continued commitment to investment in technology, EAG is the partner to keep.

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Through the years, **LingSen Precision Industries (LPI)** has emerged as a leader of semiconductor subcontract assembly in Taiwan. LPI's engineering and production teams have earned a formidable reputation worldwide for providing high-quality product lines and reliability in its total solution. LPI's assembly capabilities are proven throughout the U.S., Europe, Asia and China. The company's deliverables include micro-electromechanical system (MEMS) quad flat no-lead (QFN) packages, MEMS pressure sensors and MEMS microphones.

The MEMS QFN package is a plastic encapsulated package with exterior leads around the bottom periphery to provide short electrical connection to the printed wiring board (PWB). The package also provides excellent thermal performance by having the die attach paddle exposed on the bottom of the package surface to provide efficient heat path when soldered directly to the PWB.

The MEMS pressure sensor is a wire-bonded and lid seal on pre-mold leadframe packages, and can be used in medical instrumentation products.

The MEMS microphone is a wire-bonded and cap seal on substrate system-in-packages (SiPs), and can be used in communication and consumption products.

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MASER Engineering offers Safe Launch support to the automotive semiconductor industry. During the first ramp-up phase of new ICs in automotive applications, the manufacturer has to prove device durability. MASER Engineering supports fabless IC manufacturers with extended monitoring of the devices during Safe Launch burn-in. A dedicated setup will stress the devices beyond the observable level with ATE final test. Chips with power dissipation levels of 1 watt or beyond are exposed to a power

temperature cycling where long-term stability is proven with multiple on/off starts at very fast linear temperature ramps, up to 10 K/min. Both test methods are formulated in the dedicated automotive standard Automotive Electronics Council (AEC)-Q100. MASER Engineering is fully equipped to address all related qualification tests to this standard as a service.

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MVTS Technologies is a global full-service provider of refurbished ATE to the semiconductor industry. MVTS provides support and service for a selection of legacy Credence, LTX, Teradyne and Verigy ATE worldwide, configured and refurbished to customers' specifications. With a global team of field service representatives, MVTS is confident in providing each customer with maintenance, installations, de-installations and repairs. In addition, the company has a broad range of value-added services such as turnkey applications, subcontract printed circuit board (PCB) repair and essential test cell consumables.

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Presto Engineering, an International Organization for Standardization (ISO) 9001 company, delivers Design Success Analysis, comprehensive semiconductor test and analysis solutions to IDM and fabless companies. Operating from hubs in Silicon Valley and Europe, the company's business is focused on helping to improve the speed and predictability of new product releases.

Presto combines unique technical expertise, extensive industry experience and leading-edge ATE for system-on-chip (SoC) and radio frequency (RF), along with reliability, FIB and failure analysis/fault isolation services to offer a complete product engineering solution designed to complement customers' internal resources.

During 1H 2010, Presto established new hubs in Europe focused on failure analysis and reliability services (Normandy hub, ex-NXP lab) and ATE services, covering test program development and

engineering bring-up support for both wafer and packaged parts (Grenoble hub).

Presto is now offering specialized RF characterization and testing services from its Silicon Valley and Grenoble hub, covering wafer-level, packaged part and multichip modules (MCMs). The company's lab has the ability to use high-frequency test and measurement equipment (i.e., network analyzer, pattern generator, bit error rate test (BERT)), as well as RF ATE (Roos Instruments Cassini) supporting direct current (DC) to 100 GHz source and measure. Presto can also assist with test program development, probe card design (GGB and Cascade Pyramid) and automatic handler support. Presto's lab in Grenoble has the Verigy 93 K Pin Scale RF test equipment as well as 300 mm wafer probe support.

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STATS ChipPAC's low-cost flip-chip (LCFC) technology utilizes copper column bump to deliver a powerful packaging solution at a dramatically reduced cost. LCFC technology delivers flip-chip packages at price points below wire-bond packaging due to its innovative routing-efficient interconnection structure, simplified substrate design and cost-effective mold underfill process. The unique structure of LCFC when combined with copper column bump achieves an even lower cost solution with higher routing densities and is scalable to finer bump pitches. Copper column bumps enable a higher I/O density with a much finer pitch between the columns than standard solder bumps, along with a higher resistance to electromigration. Although copper column is a hard bump material that can typically cause damage to low-K (ELK) layers in finer silicon nodes, the LCFC interconnect structure dramatically reduces the mechanical stress on silicon subsurface layers, resulting in the elimination of the ELK damage phenomenon commonly observed in sub-45 nm silicon nodes.

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International Challenges in Environmental Compliance and Supply Chain Sustainability

Tom Krawczyk, Compliance Manager, Conexant Systems Inc.
Bob Warren, Director, Packaging Engineering & Assembly Manufacturing, Conexant Systems Inc.

F ive years ago, if you asked someone in the electronics industry to explain the meaning of "environmental compliance," the answer would have been fairly straightforward. Environmental compliance meant meeting the European Union's (EU) recycling requirements identified in the Waste Electrical and Electronic Equipment (WEEE) directive and meeting the EU's substance/threshold limit requirements of the Restriction of Hazardous Substances (RoHS) directive which took effect on July 1, 2006. The environmental management standard of record was the relatively well-known International Organization for Standardization (ISO)14000:1996.

Fast forward to 2010 and ask the same question, and the answer is entirely more complex and difficult. Today, environmental compliance is not solved by crossing a well-defined finish line. Over the past few years, there has been an explosion of new environmental requirements across the globe, with a myriad of new restrictions and reporting requirements being imposed on the entire electronic supply chain. Many of these regulations are still evolving, most are widening in scope, and some are interpreted or enforced differently in various global regions. In addition to regulations, there are additional requirements being imposed by large original equipment manufacturers (OEMs) that are often more rigid and extensive than those being pushed by governmental agencies. All of this is forcing electronics companies and their suppliers to deal with an overwhelming set of environmental compliance variables that vary from customer to customer, product line to product line and region to region.

An Explosive Growth of New Regulations

It has been said that the massive number of new environmental regulations that are coming into force can be best described as a tsunami—many are coming in from distant shores, often with little warning. To understand the magnitude of dealing with environmental compliance today, consider what has happened in the last few years:

- China introduces their version of RoHS adding new labeling requirements and environmentally friendly use period (EFUP) rules, which specify the period of time before any of the RoHS substances are likely to leak out and cause possible harm to health and the environment.
- California introduces their own RoHS laws prohibiting an electronic device from being sold or offered for sale in California

if that device is prohibited from being sold or offered for sale in the EU due to the presence of lead, mercury, cadmium or hexavalent chromium above certain maximum concentration values (MCVs).

- ISO releases an amended version of its environmental management standard ISO14001:2004.
- The EU introduces Registration, Evaluation, Authorization and Restriction of Chemical Substances (REACH), ultimately regulating an estimated 30,000 chemicals and banning or restricting any substances of very high concern (SVHC). Several revisions have already been made to the SVHC list of chemicals/compounds. There are currently a few dozen SVHCs for semiconductor "articles," but the list is expected to grow to 300 or more.
- Joint Industry Guide (JIG)-101 significantly grows the number of reportable substances in the Material Composition Declaration for Electronic Products.
- Japan introduces the Japan Green Procurement Survey Standardization Initiative (JGPSSI) standardizing the list of substances identified by the JIG and establishing new and comprehensive chemical management systems requirements. Although the requirements were considered voluntary, many Japanese customers now require their upstream suppliers to adapt and push the Japanese chemical management systems requirements throughout their supply chain.
- Carbon, Greenhouse Gas (GHG) Protocol and energy content reporting requirements begin expanding.
- The EU begins drafting RoHS 2, which will restrict additional hazardous substances and will expand the scope of the directive to include previously exempted categories 8 and 9 (medical devices and monitoring and control instruments) with coverage effective January 1, 2014.

If the numerous known and pending environmental regulations weren't enough for companies to deal with, new social responsibility issues are now becoming regulatory targets. The sweatshop conditions that started in the apparel business in emerging countries are now being seen in the electronics industry, as evidenced by the recent and much publicized news of suicides amongst electronics assembly workers in China. Attempts to rectify these conditions include:

- Establishment of the Electronic Industry Citizenship Coalition (EICC) to promote a common code of conduct for the electronics and information and communications technology industries. Members such as Apple, Cisco, Dell, Intel, HP and others are members of this coalition who are working to improve environmental and worker conditions. EICC member companies promote and sometimes require their suppliers to adopt corporate social responsibility (CSR) programs.

- Introduction of the Conflict Minerals Trade Act, which is legislation designed to help stop the deadly conflict over minerals in eastern Congo by regulating the importation and trade of tin, tungsten and tantalum—minerals commonly used in cell phones, laptop computers and other popular electronic devices. Under the bill, U.S.-sanctioned auditors would audit mineral mines declaring them conflict-free or not. Importers of these goods would have to certify on their customs declaration whether their goods were conflict mineral-free based upon this audit system.

Treating Compliance as an Ongoing Process

After exerting tremendous effort to comply with RoHS and WEEE, electronics companies are now finding that developing sustainable, environmentally friendly products is an ongoing process and not a one-time effort. The challenges in ensuring product compliance seem overwhelming (Figure 1), especially for small to mid-sized companies, and it appears it is only going to get worse. After RoHS 2 is enacted into legislation in the next couple of years, it appears that RoHS may become a "Conformité Européene (CE) Mark" directive. The CE marking certifies that a product has met EU consumer health, safety and environmental requirements. Manufacturers and anyone selling the product under their brand will have to audit their manufacturing processes or subcontractor's processes and have the documentation to prove that their products do not have any hazardous substances. Furthermore, this documentation will need to be retained for 10 years. Needless to say, it appears that environmental compliance will be a much more complex and resource-intensive activity in the future.

Figure 1. Challenges in Ensuring Environmental Compliance

How do companies with limited resources, especially after shedding resources to survive the recent economic downturn, meet all of these compliance demands in a cost-effective way? Certainly, reacting to each new regulation or iteration and treating them as separate events will be costly, time consuming and will never allow a company to get ahead of the curve. Staying in reactive mode also increases potential market risks, such as costly and time-consuming redesigns, product recalls, lost sales and brand damage. What is needed is a systematic approach, which provides a way to be compliant, reduce market risk and do it at a lower cost than competitors.

From a high-level view, there are four key areas that most companies need to focus on to build an effective and sustainable environmental compliance program (Figure 2).

Figure 2. Focus Areas for Environmental Compliance

Understanding Compliance Requirements

While few companies can devote the amount of resources to compliance management that large OEMs can, smaller companies can always establish cross-functional teams comprised of members from the engineering, manufacturing, legal, procurement and sales departments. Each team member can represent their functional group and work together to collectively understand requirements, address short-term goals and establish systems and processes to meet long-term goals.

Staying on top of changing and emerging environmental initiatives, directives and regulations is challenging even for experienced compliance managers. One way of accomplishing this is by monitoring information available to the public on various Web sites. There are also industry-specific professional societies, trade associations and consortiums that provide reports, workshops, conferences and guidance. Another tool is to use subscription-based Web services that deliver information on product-oriented environmental compliance for the electronics industries through online tools, webinars, electronic newsletters, etc. Some downstream customers will also inform their supply chain of pending changes, and some even offer workshops for their suppliers to help them understand changes and ways to become compliant.

Design for Environment

One of the best ways to develop sustainable product is to design compliance into the products right from the beginning, commonly called design for environment (DfE) (Figure 3). The first step is to specify all the requirements necessary to produce an Environmentally Preferred Product (EPP) in the marketing specification. The marketing specification should detail the use of non-hazardous materials and the maximum power consumption to meet energy efficiency requirements, and address any end-of-life reuse or recycling requirements. Making compliance data available to designers throughout the design process will also help ensure that the materials and components selected are compliant. Addressing compliance early while design flexibility is still high allows engineers to use materials that provide good performance, are environmentally friendly, and avoid costly re-engineering and late product launches. Good DfE practices also involve selection of environmentally friendly shipping

E-System Design released Sphinx for Signoff, the company's signal and power integrity co-simulator, at Design Automation Conference (DAC) 2010. Over the past year, numerous customers have validated Sphinx's accuracy and simulation run times on advanced and complex structures that other commercial tools could not perform. Additional features include support for Windows 32/64 bit; support for DXF, MCM, BRD and SiP file formats; performance of quick "what if" analysis within Sphinx; support for vendors' capacitor libraries; viewing of meshed design before simulation, removing any doubt about what is being analyzed; scripting to achieve faster turnaround time for common operations; and performance of time domain analysis with an integrated and proven flow using IdEM Plus.

In addition, a new prototype tool for 3-D packaging structures (supporting all interconnects, wire bonds and through-silicon vias (TSVs)) capable of accurately extracting hundreds of interconnects was announced.

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ICsense is an IC design house with core competence in analog, mixed-signal and high-voltage IC design. ICsense offers design services starting from building block design up to complete turnkey application-specific IC (ASIC)/system-on-chip (SoC) solutions, excelling the state-of-the-art for the automotive, medical, industrial and consumer markets. The company delivers innovation and high complexity at reduced risk, and its mission is to be the number one partner for innovative mixed-signal and high-voltage IC developments. ICsense offers high quality through a highly skilled expert engineering team, a structured IC design methodology, International Organization for Standardization (ISO) 9001:2000 certified quality procedures and close cooperation with its customers and partners.

ICsense has key IC design experience in power management, high-voltage IC design, drivers, microelectromechanical systems (MEMS), sensor and actuator interfacing ICs, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), timing circuits and ultra low-power design.

ICsense provides customer-specific ASIC turnkey solutions from idea to final product, including feasibility study, system definition and modeling, design, layout, prototyping, prototype testing, production test and assembly coordination.

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Mentor Graphics released three new products for IC physical design in Q2 2010. The Calibre InRoute design and verification platform enables designers to natively invoke Calibre tools within the Mentor Olympus-SoC place-and-route system to achieve true manufacturing closure during physical design. It significantly reduces time to closure by automatically detecting and fixing design rule checking (DRC) violations and making design-for-manufacturing (DFM) enhancements while optimizing for area, timing, power and signal integrity.

Calibre xACT 3-D is a new parasitic RC extraction solution that solves the traditional dilemma of extraction accuracy versus performance by providing a true deterministic field solver with the performance of rule-based production extraction tools. The tool provides accuracy within 5 percent and runtime at least two orders of magnitude faster than traditional field solvers.

Calibre Pattern Matching replaces lengthy and multi-operational text-based design rules with an automated visual geometry capture and compare process that significantly reduces rule deck size and improves congruence between the original intent of the design specification and its implementation.

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MIPS Technologies is the embedded processor leader in the digital home with a strong presence in networking. Now MIPS is entering the mobile handset market enabled by two main inflection points: Android and 4G. Previously there was a barrier to entry for MIPS in mobile handsets because the operating system (OS) was tied to the processor, but Android removes that barrier. And since consumers now expect access to high-definition (HD) multimedia content anywhere, anytime and from any source, high-bandwidth 4G data networks are needed to move content rapidly between devices. The MIPS architecture excels at moving large amounts of data quickly. Since MIPS cores are small, more of them can fit on a die—three multi-threaded MIPS cores can fit into the area of two single-threaded cores from the competition! This leads to increased performance at lower power consumption—a necessity for next-generation mobile designs. MIPS is engaging with key providers of software, middleware and complementary intellectual property (IP) to provide customers with choices and design differentiation. Based on recent design wins, MIPS-based mobile handset chips should arrive in 2011.

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Mixel, the leader in mobile mixed-signal IP, announced the availability of MXL-SRDS-SGMII, a Serial Gigabit Media Independent Interface (SGMII) serializer/deserializer (SerDes) implemented in digital CMOS technology. The SerDes IP offers a data transfer rate of 1.25 Gbps for both upstream and downstream direction, meeting the Cisco GMII standard.

Mixel is a leading provider of mixel-signal IP cores to the semiconductor and electronics industries. Mixel's mixed-signal IP portfolio includes high-performance physical layers (PHYs), SerDes, transceivers, phase-locked loops (PLLs), delay-locked loops (DLLs) and analog building blocks, which are used in mobile applications such as Mobile Industry Processor Interface (MIPI), Mobile Display Digital Interface (MDDI), networking and storage.

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Novocell Semiconductor is the reliability leader in antifuse non-volatile memory (NVM) products and the only supplier of 2nTP, the first multi-time write antifuse device. Novocell's SmartBit technology allows 2nTP to be programmed two, four or eight times while saving users approximately 60 percent of the area used when cascading multiple one-time programmable (OTP) memory blocks. This month Novocell is releasing an enhanced version of its silicon-proven NovoBlox OTP technology. This release provides a high-density solution with significant area reductions. The enhanced blocks for a comparable size will be four times denser than the original NovoBlox—a 70 percent smaller footprint.

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Oracle provides industry-leading business solutions for the semiconductor industry based on best-of-breed applications; middleware; and open, standards-based technology. Oracle's supply chain solution helps semiconductor companies achieve accurate consensus forecasts, optimized inventory leveling and postponement strategies, faster planning cycles and superior on-time delivery.

Oracle helps synchronize customers' entire supply chain by providing real-time engineering and bill of materials (BOM) changes to suppliers and design partners, and a central repository for all product data providing access through supplier portals. Workflows for approval and sign-off between various departments and supply chain partners are automated and help eliminate supply chain errors often caused by manual processes to update product information. Oracle will also help improve a company's quality management program and help keep track of supplier and manufacturing partner key performance indicators (KPIs) through its analytics.

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Rapid Bridge is an innovator in advanced semiconductor design and development processes with a unique approach to addressing the industry's issues of cost, performance, power and time-to-market. The company's disruptive, game-changing technologies and solutions create exceptional value for customers by enabling them to lead the next-generation silicon products.

Rapid Bridge's liquid product family—LiquidIP, LiquidASIC and LiquidSoC—leverages its proprietary Global Shared Resources Architecture to deliver IP and IC designs that are among the smallest, lowest power and best-performing solutions available. Their liquid or metal-programmable products offer customers greater flexibility for design changes or derivative products with significantly reduced costs and time-to-market.

Rapid Bridge's revolutionary core power reduction (CPR) is a matchless solution for improving power, performance and area (PPA) metrics for complex SoC designs. Unlike other approaches, CPR technology improves all PPA components concurrently—without tradeoffs.

Rapid Bridges Design Services Division is a global leader in cutting-edge IC design technology with extensive, proven experience delivering complex multi-million gate chip designs targeted to multiple deep submicron technologies.

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Serus has added new features in its flagship Intelligent Operations Management (IOM) suite of products that enable companies to deal with the current extension of supply cycle times due to supplier allocations. These allocations, in turn, are requiring companies to manage customer fulfillment using exceptions processes. The new features in Serus IOM allow companies to manage this situation more efficiently across the spectrum of processes that are impacted—front-end and back-end manufacturing, quality engineering and order fulfillment. Key additions were supplier on-boarding—the ability to fully integrate suppliers within weeks; tactical planning—wafer to fulfillment lot level tactical supply chain planning capabilities with scenario comparison, rapid planning, integrated real-time supply visibility, multi-level binning/downgrading optimization, consumable/durable planning, projected cost/margin and integrated order promising capabilities; and integrated manufacturing and engineering data management with supplier/factory systems—no-touch synchronization of manufacturing specifications with integrated engineering change order (ECO) across internal and supplier master data systems, improving manufacturing quality, reducing waste and decreasing cycle times. Drawing on its years of experience in the semiconductor industry, Serus continues to innovate and extend its suite of products to adapt to the changing circumstances.

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Sidense provides secure, very dense and reliable non-volatile OTP memory IP for use in standard-logic CMOS processes with no additional masks or process steps required and no impact on product yield. The company's innovative one-transistor (1T)-Fuse architecture provides the industry's smallest footprint, most reliable and lowest power logic NVM IP solution. With over 60 patents granted or pending, Sidense OTP provides a field-programmable alternative solution to Flash, mask read-only memory (ROM) and eFuse in many OTP and multi-time programmable (MTP) applications.

Sidense OTP memory is available from 180 nm down to 40 nm, and is scalable to 28 nm and below. The IP is offered at and has been adopted by top-tier semiconductor foundries and selected integrated device manufacturers (IDMs) for precision analog trimming, code storage, encryption keys such as High-bandwidth Digital Content Protection (HDCP), radio frequency identification (RFID) and chip ID, medical, automotive, and configurable processors and logic.

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Whizz Systems is an engineering and manufacturing services company headquartered in Silicon Valley, California. The company announced expansion to its facility by acquiring a new 60,000 square foot building and adding new surface mount technology (SMT) lines to service their increasing demand. The company sees a new trend in offshoring specifically for new product introduction (NPI), and companies desiring to keep their prototyping and design for manufacturability (DFM) close to their homeland.

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What's Your Return on Development? Identifying the Key Levers and Moving the Needle

Mark Davis, Principal, Deloitte Consulting LLP
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For the semiconductor industry, the ability to achieve business goals corresponds to constant focus on new products. This is, after all, an industry that has made an art of monetizing the "learning curve." But the relentless pace of product innovation creates enormous pressure to manage the development pipeline with speed and rigor. In the end, the new product portfolio must generate compelling value and continue to fund an increasingly costly development process. Is your company adeptly managing all the moving parts of the development machine, and is it accurately measuring the performance factors needed to achieve financial growth?

As the costs of bringing new products to market continue to grow exponentially, semiconductor companies are finding they need to shift to a new performance curve to innovate, grow, and increase revenue and earnings.

Figure 1. Increasing Costs of Semiconductor Product Development

"It costs a new venture at least $15 million to reach tape-out. Such high initial investment is too steep for a venture investor unless there was a good probability of a really huge return. There is no value to the venture investor in putting $25 million into a company to achieve a $50 million exit."

— Lip-Bu Tan, Chairman, Walden International

Source: Synopsys, 2008

Based on Deloitte's work and recent benchmarks, we have identified key drivers and improvement actions that are the primary levers of overall "return on development" (RoD). RoD is a metric that allows companies to track their performance over time and measure it against other companies. Pull these levers correctly for your specific business situation and you stand a greater chance of reaping the rewards of new product development.

Armed with a solid understanding of how to address the components of RoD, these key factors of product development—engineering effectiveness, portfolio optimization and time-to-market—all converge in a stage-gate framework that sustains the focus on project performance, enables informed decision making and drives accountability for delivering "big picture" results.

Product Development and the Importance of Margin Pools

Product development aims to exploit candidate market areas that represent attractive margin pools—areas of customer demand that seem to command a desirable premium over the cost of accessing them.

Margin pools are a function of market size and the gap between the prevailing price and the cost to service the demand. In the semiconductor industry, technology's constant learning curve steadily opens up new margin pools, both by increasing the gap between price and cost, and by introducing new features and capabilities which widen and deepen the market's appetite. Advances in low-power computing and 3-D graphics are a prime example. The smartphone boom accelerated when the power of handheld devices passed a tipping point, expanding into a wider, mainstream audience and exploiting consumer features along with the business capabilities—notably e-mail—of prior generations.

At the same time, the cost of defining, designing and delivering products to tap into those margin pools is increasing. The exponential
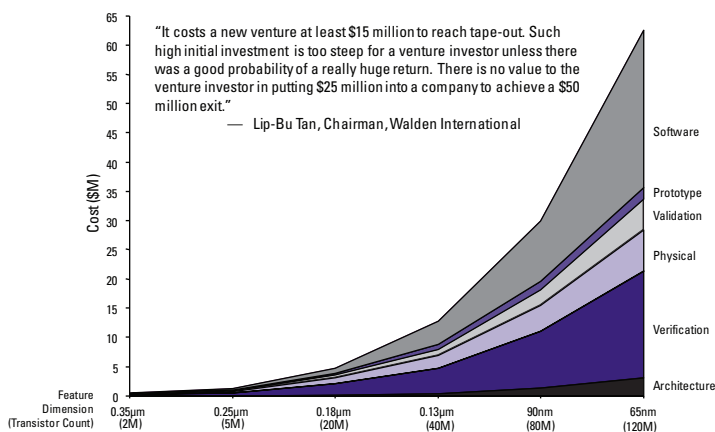
increase in development cost previously described continues through 40 nanometers and beyond, yet at the same time the unavoidable uncertainty about "if, when and how big" pervades the entire go-to-market process. Ultimately, though, the bets placed in product development must fund the whole enterprise. The overall gross margin pool (money left over after the cost of the goods is accounted for) must pay for the rest of operations, selling and administration, and sustain ongoing development efforts that will produce future generations.

For companies on a steep growth trajectory, this forward investment must reflect future, not current, business magnitude. So the bar is set very high for how big a margin pool is needed to achieve business objectives. Implementing an RoD framework helps a company identify where it is performing well and where it most stands to benefit from "moving the needle."

The Metrics of RoD

RoD is defined as the net present value (NPV) ratio of gross margin produced to the corresponding investment in product development. It is an intuitive, effective and concise yardstick for judging the financial merits (or results) of a development effort.

For example, if your RoD is 3 (3:1), the gross margin "harvest" of your development investment is triple that investment, in present dollar terms.

So the components of RoD are:

- The price-volume curve that the product or service commands in the marketplace (and where your company decides to land on it).

- How much money you are investing to develop the saleable product or service in question.

- The cost of producing and delivering each unit of the product or service.

- The points in time where these monies are moving in and out of the enterprise.

- The company's cost of capital.

Now, how can you improve this metric, despite trends in increasing development costs, product life cycle compression, and more aggressive competition and margin erosion? What are the levers you can pull?

Portfolio and Pricing

Choosing a portfolio of products to develop with the right price, volume and technology is, of course, paramount. The margin pools you select to tap and how well they are chosen is critical. Their interactions with your company's existing product set, their influence on end-to-end development cost, and the degree to which they are accessible or coveted by others can all affect RoD. But the reality is that these also change over time, so your company's ability to track, adapt and reshape its portfolio—especially with respect to products still in the pipeline—is key.

Product Cost

The design locks in 90 percent of product cost, although sourcing and operational wizardry can be tweaked in various places. Establishing design cost targets is the key way of influencing this.

Development Cost

Development cost is always an area of major contention. One key point is that development monies are spent on both the winners and the losers. There is tremendous leverage in selecting the highest probability efforts to work on in the first place—and smartly cutting losses when future prospects start to fade.

The other key area of development cost lies in individual and collective engineering effectiveness. In many companies, hard-to-find engineering talent spends too much time locked in tasks and activities that don't contribute to product development progress, but instead are artifacts of inefficient development processes and organizations.

Time

Time-to-market is not just a competitive question; if your development process takes too long, the revenue dollars that ultimately roll in are nearly worthless compared to the development spend incurred.

Figure 2. Revenue Loss for Being Late to Market
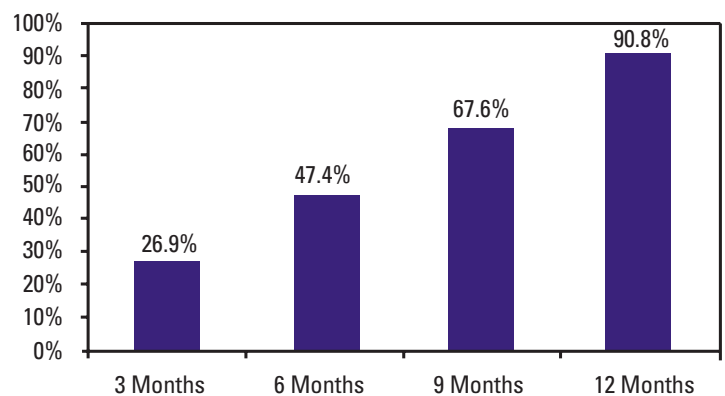
Source: IBS, 2007

Cost of Capital

Take cost of capital as a given. Weighted average cost of capital (WACC) is useful as a tool to take time out of the equation and put today's spend and tomorrow's margin on a level playing field in terms of impact to the company.

Raising the Bar on Product Development Performance

Once a company puts RoD into play and has specific metrics for measuring current performance, it becomes a matter of utilizing effective management techniques, processes and other metrics to jumpstart product development performance. The following includes some of the most effective ways in which leading companies raise the bar to achieve their goals:

Portfolio and Development ROI Metrics

There's inconsistency in how companies approach development financials. The tiered nature of semiconductor development, where individual projects often share "core" intellectual property (IP) and platforms whose development costs are meant to be amortized across multiple end products or families, can be frustratingly ambiguous. This sometimes results in the participants backing off from the controversies that can arise from trying to model and apply tests of financial return. Consequently, many companies

GLOBAL MARKET TRENDS

ASIA

>53% – Asia's projected share of the global closed-circuit television (CCTV) market by the end of 2013. – *RNCOS*

35% – Year-over-year (YoY) growth of the Asia-Pacific PC market in Q2 2010. – *International Data Corporation (IDC)*

$279 million – Revenue generated by the Asia-Pacific electronic design automation (EDA) industry in Q1 2010, a 33.2% YoY increase. – *EDA Consortium*

$22 billion – Expected value of China's automotive electronics market by 2017. The drivers of this growth include increased penetration of automotives within the region and the aggressive overseas expansion plans of China automotive makers. – *IMS Research*

12 – Number of clean technology initial public offerings (IPOs) that occurred in China in Q2 2010, out of a total of 19. – *The Cleantech Group and Deloitte*

59 million – Forecasted number of flat-panel TV unit shipments in China in 2014, growing at a compound annual growth rate (CAGR) of 14% from 31 million in 2009. – *DisplaySearch*

15 million – Estimated number of cars that China will produce this year, an increase from 11 million in 2009. This rapid growth is due to the region's increased production, developing technologies, top-level and regional planning of automotive factories, financial resources, and the spending power of its growing middle class. – *International Organization of Motorvehicle Manufacturers*

15% – Japanese companies' current share of the global semiconductor market. The region holds less than 10% of the global liquid crystal display (LCD) market. – *Wataru Izumiya, Senior Executive Managing Director, Sangyo Times*

188% – Projected growth of chip equipment sales in South Korea in 2010, reaching $7.5 billion. – *Semiconductor Equipment and Materials International (SEMI)*

$5.7 billion – Value of 217 approved Taiwan-based business projects that will invest in China in 1H 2010. The number and value of the projects increased 174.7% and 195.8% YoY, respectively. – *Taiwan's Ministry of Economic Affairs (MOEA)*

51.6% – Estimated increase in Taiwan's small- to medium-sized panel shipments in 2010. Cell panel orders from Korea-based vendors are expected to account for 12% of the total small- to medium-sized panel shipments from Taiwan in 2010. – *Digitimes Research*

$34.2 billion – Value of export orders received by Taiwan in June 2010, historically the second-highest figure with growth of 1.5% month-over-month (MoM) and 22.5% YoY. – *MOEA*

77.6 million – Number of network interface cards (NICs) that Taiwan-based wireless local area network (WLAN) product makers shipped in Q2 2010. – *Digitimes Research*

80% – Forecasted growth of Southeast Asia's semiconductor equipment market in 2010. – *SEMI*

$437 million – Investment made in the Philippines' electronics industry during the first five months of 2010, increasing more than 10 times YoY. – *Semiconductor and Electronics Industries of the Philippines Inc.*

INDIA

$40 billion – Forecasted investment made in India's telecom sector in 2010, an increase of 100% from last year. The significant increase in foreign investment is driven by different segments of the Indian telecom industry such as mobile and broadband, possessing huge potential for future growth. – *Telecom Equipment and Services Export Promotion Council (TEPC)*

27.3% – Expected growth of mobile connections in India in 2010, reaching greater than 660 million. Mobile service revenue in India will reach $19.8 billion by the end of the year, up 19.7% from 2009. – *Gartner*

$8 billion – Forecasted value of India's semiconductor market by the end of 2011. By the end of this year, the country's share of the global semiconductor market is estimated to reach 2.3%, making India one of the fastest growing semiconductor markets in the world. – *India Semiconductor Association (ISA) and Frost & Sullivan*

16% – Forecasted CAGR of India's navigation and telematics system market for the period 2010 to 2013, reaching around $48 million by 2013. – *RNCOS*

$37 billion – Estimated total available market of India's electronics industry in 2011, rising from its current value of $25 billion. – *ISA*

$1.6 billion – Estimated revenue of the cathode ray tube (CRT) TV market in India in 2011, down 32.3% from $2.3 billion in 2010. In contrast, LCD TV revenue will rise to $3.5 billion in 2011, increasing 94.3% from $1.8 billion in 2010. – *iSuppli*

275 million – Predicted number of high-speed Internet users in India by 2015, as telecom firms roll out Broadband Wireless Access (BWA) air waves that were auctioned in June. – *Associated Chambers of Commerce and Industry of India (ASSOCHAM) and Frost & Sullivan*

>30% – Anticipated CAGR of India's CCTV market between 2010 and 2013. Increasing terrorist activities and attacks have created strong demand for advanced safety and security solutions. – *RNCOS*

15% – Expected CAGR of auto component production in India by 2014. Increasing demand from the country's automobile industry and surging exports will drive this growth. – *RNCOS*

EUROPE, THE MIDDLE EAST AND AFRICA (EMEA)

24% – Europe and Israel's share of global clean technology investment deals in Q2 2010. North America accounted for 72%, raising $1.5 billion; India accounted for 3%; and China for nearly 2%. – *The Cleantech Group and Deloitte*

45% – Europe's projected share of the global Internet Protocol (IP) TV market by 2014. Asia, North America and other regions will follow at 31%, 19% and about 5%, respectively. – *Multimedia Research Group*

$3.2 billion – European semiconductor sales in May 2010, a 43.8% YoY increase. – *European Semiconductor Industry Association (ESIA)*

7.3 million – Number of cars registered in the European Union in 1H 2010, a 0.2% increase from the same period in 2009 but a 10.3% drop from 2008. – *European Automobile Manufacturers Association (ACEA)*

21.1% – YoY growth of the PC market in the EMEA region in Q2 2010, with close to 24 million PCs shipped. – *IDC*

$224.2 million – Revenue generated by the EDA industry in the EMEA region in Q1 2010, up 0.5% YoY. – *EDA Consortium*

4.6 million – Expected number of portable navigation device (PND) shipments in Western Europe in 2014, up from 388,000 in 2009. – *iSuppli*

40% – Expected CAGR of the number of mobile TV subscribers in Germany between 2010 and 2013. The roll out of advanced technologies such as 3G and 4G have been driving the growth of the country's mobile TV forecast. – *RNCOS*

32% – Percentage of Europe's venture capital (VC) investment that went into UK-based companies in Q2 2010. – *Dow Jones VentureSource*

17.9% – Forecasted CAGR of the installed base of smart electricity meters in Europe between 2009 and 2015, reaching 111.4 million at the end of the period. – *Berg Insight*

THE AMERICAS

$1.2 billion – Estimated amount of spending on mobile display ads in the U.S. in 2015, nearly quadrupling from just under $313 million today. – *ABI Research*

$1.7 billion – Value of orders posted by North America-based semiconductor equipment manufacturers in June 2010. – *SEMI*

35% – Forecasted growth of chip equipment sales in North America in 2010, reaching $4.6 billion. – *SEMI*

$3.8 billion – Value of 369 funding deals in California in Q2 2010, an increase from 299 deals valued at $2.2 billion in Q1 2010. – *PricewaterhouseCoopers/National Venture Capital Association (NVCA) MoneyTree Report*

>90% – Percentage of U.S. survey respondents, as well as VCs in Europe and Canada, that expect the number of venture firms to decrease between now and 2015, while a majority of venture capitalists in China, India and Brazil anticipate adding more venture firms in their regions during the same time frame. – *2010 Global Venture Capital Survey by Deloitte and NVCA*

25 million – Forecasted number of Internet-connected TV shipments in North America in 2010. – *DisplaySearch*

$492.9 million – Value of EDA products and services purchased by the Americas in Q1 2010, a decrease of 0.2% compared to Q1 2009. – *EDA Consortium*

18% – Penetration rate of standalone Blu-ray players among TV-owning households in North America, up from just over 7% in 2009. – *ABI Research*

70% – Percentage of U.S. gross domestic product (GDP) accounted for by personal consumption, much of which is related to electronic products. Personal consumption accounts for 60% of Japan's GDP. – *iSuppli*

20 – IPO pricings in the U.S. technology sector in the first six months of 2010, compared to six in 1H 2009. – *Updata Advisors*

2 million – Forecasted number of 3-D TVs shipped in North America this year. – *DisplaySearch* ∎

Getting the Most out of a Yield Management System

Nancy K. Tsai, President, Nancy K. Tsai Consulting

A key prerequisite for success in yield management system (YMS) implementation is that management at the implementing company broadly understands the nature of the upfront work required and supports it by empowering an YMS administrator who can enlist support from various parts of the company before and during the implementation process. As will be described in detail in the remainder of this article, the YMS administrator will need help from various groups of people: potential YMS users, mainly production and engineering staff; the information technology (IT) group; the enterprise resource planning/manufacturing execution systems (ERP/MES) database manager; and the test suppliers that provide the incoming raw datalogs and test summaries. (If a company has purchased a complete design-to-yield management system, then the design group should also participate in the implementation process.)

At the most general level, the challenge of YMS implementation is to correctly translate the diverse data inputs from a fabless or fab-lite production testing process into information stored in a unified YMS database. These inputs could include test datalogs, unprocessed data from parametric measurements such as wafer electrical testing, or test operations such as wafer sort, final test or module test. They could also include yield summaries—the binning summary files collected at test operations. The data format of these inputs can vary by data type—the unique combination of tester platform and operation in which the datalogs or yield summaries are generated. Most companies today also link the genealogy data for each lot—essentially a lot movement and process history extracted from the company's ERP and/or MES databases—to its test and yield database.

Customized parsers in the YMS data processing module extract the desired information from these datalogs and yield summaries and convert them into the native YMS format so they can be loaded into the YMS database. Parsers are generally created by the YMS software company in response to guidance from the implementing company. However, it is also extremely beneficial for the implementing company to have some capability to write its own software routines for pre- or post-processing of test and yield data, or to convert raw data into the native YMS format.

These upfront steps to accommodate and integrate diverse data inputs in a robust way are critical to the success of yield analysis with YMS,[1] but they are often neglected. The rest of this article will describe how an YMS administrator can engage with the different players involved in implementation to successfully accomplish these key tasks. This article seeks to serve as a kind of checklist for YMS administrators embarking on an YMS implementation, a guide for involved company staff on how they can help during the implementation process and an overview for managers on the types of support for implementation that they need to ensure within the company.

Involving Prospective YMS Software Users

The "customers" for YMS should play a key upfront role in YMS implementation, starting by helping the YMS administrator understand the data conversions that will be needed (and how the number of such conversions can be minimized[2]). To this end, the prospective YMS users should provide sample datalogs and yield summaries to their YMS administrator and parser development team (based in-house or at the YMS vendor), along with a list of information they expect to be parsed for each data type and samples of the analyses they wish to perform. It is particularly important to include "bad" datasets (i.e., ones with known format issues) to test the parser guidelines for rejecting data.

The users need to remain engaged throughout the parser development process to ensure that subtleties in data formats are correctly and efficiently treated. For example, users may be able to communicate to the parser developer that the "lot number" field from test supplier A and the "lot ID" field from test supplier B should both be treated equivalently as wafer lot numbers. Prospective users can also provide timely notice of upcoming process changes that will need to be handled by the YMS such as changes to the final test retest flow for a product.

A staged implementation of the YMS by data type facilitates early adoption by users and allows user feedback to be incorporated as efficiently as possible. When several types of data will all be stored into the YMS, the users and administrator should determine a priority list for implementation of the various data types. Users should then be encouraged to start using the YMS software when data for the first data type is available, communicating to the YMS administrator any errors they find in the data or any problems in analyzing the data the way they expected. This prevents the same mistakes from being propagated to each subsequent data type. Early

involvement in a staggered implementation process allows users to focus on characteristic problems associated with each data type. For example, a key concern at the wafer sort operation may be the ability to furnish an accurate composite map, while for final test it may be most important to verify the retest-recombined yield calculation and retest code input accuracy.

Involving IT

Beyond the obvious role of the implementing company's IT staff in providing hardware maintenance service as needed for an enterprise YMS, there are a number of more specific ways that an IT staff can help ensure the success of a YMS implementation. First, they can work proactively with the YMS administrator, corporate planning and quality assurance staff, and YMS users to define and put in place a back-up and archiving strategy that avoids any interruption to the availability of the YMS tool or the data. For example, maintaining excessive active data tends to degrade system performance, but not keeping enough data active delays data retrieval for older products, as would be needed to evaluate returned materials authorization (RMA) units.

Second, the IT group can help by setting up alert features that flag abnormal system behavior or errors. The YMS software itself can generally alert users to data that failed processing in some way, but broader failures such as problems with a transfer link to the test vendor's ftp site may not be caught by the YMS tool.

Third, IT personnel have a critical role in setting up a reliable data transfer protocol with the test supplier. In implementing an YMS, automating the collection of incoming datalogs is a must. A common method is using an automatic script that performs the file transfer,[3] ideally in a way that allows quick isolation of any problems with incoming data for a particular data type.[4] An IT staff with sufficient resources and experience may be able to write these scripts themselves, or the company may need to rely on the YMS vendor's technical support staff.

Involving Logistics Database Managers

Extracting the lot genealogy data from a company's logistics databases (MES and/or ERP tools) and adding it to the lot's yield and test data in the YMS database enhances the ability of engineers to pinpoint the source of any yield problem. However, the method of incorporating such information can vary significantly from one company to another and thus depend on close collaboration between the YMS administrator, YMS vendor (who may need to customize the YMS tool), and database managers for the MES and/or ERP systems. These database managers will need to provide the links to the correct lot history tables in a timely manner and also make sure that the YMS manager is alerted to any changes in the MES and/or ERP databases. Ongoing involvement of these database managers will help avoid unpleasant surprises in the form of scripts that must be laboriously rewritten or YMS output that suddenly becomes inaccurate or non-functional.

Coordinating YMS Implementation with Test Suppliers

The YMS administrator cannot deeply understand his or her YMS and its possible failure modes without having a strong grasp of test floor setup and operations. Production semiconductor testing still requires human operators to perform various data input tasks during the testing process, with a high potential for errors. The

YMS administrator (and ideally users) should understand these vulnerabilities at the test supplier[5] and, where possible, work with the supplier to automate the data input for the test environment variables and setup information. Where errors are likely but automation is not possible or advisable, the YMS administrator should work with the supplier to set up formalized data logging instructions that help minimize the risks of operator error. This is very much an interactive process that needs supplier input. For example, instead of proposing a customized set of retest codes for final test, the company might minimize errors by using the test vendor's default set of retest codes where applicable and only developing new retest codes where the vendor's codes fall short. These jointly developed data logging procedures should be codified in a written specification.

During YMS implementation and thereafter, the YMS administrator needs to periodically feed back to each test supplier information about the quality of their incoming data as well as the robustness of the data transfer process originally established for each supplier (see section "Involving IT"). For an YMS tool to be useful in production yield management, this review should be part of the customer's supplier quality assessment process.
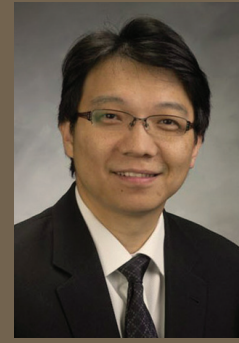
Other Skills for the YMS Administrator

The previous sections of this article have focused on the YMS administrator's role as a point person to pull in the resources and knowledge of the different players that must contribute to the success of an YMS; equally important is for the YMS administrator to become well-versed in the intricacies of actually using the YMS. In this way, he or she can enhance the support by the YMS vendor. An YMS administrator who is very familiar with the client interface for the YMS software can help users distinguish genuine system bugs from momentary roadblocks caused by user inexperience. Beyond this, the administrator should learn more sophisticated skills that will help him or her spot yield management problems and correct them. The YMS administrator should learn from the YMS supplier how to trace a dataset back to its raw datalog(s) to identify problems, and then how to manually remove the resulting problematic dataset and replace it with a correct one. (For customers that collect datalogs in the standard test/Teradyne data format (STDF), in particular, it is worthwhile to have and use a standalone STDF viewer, as a number of common problems can be cleared up by examining the raw STDF files.) In collaboration with the YMS vendor, the administrator should develop a method for cleaning up portions of the YMS database, either through direct manipulations to the database or by means of a dedicated software tool, if the tool's client interface does not allow the administrator to perform this task. Being conversant with the data loading process can also allow the administrator to override an established data loading script to fulfill a user's high-priority request (e.g., to provide data for a report analyzing an urgent yield problem). Finally, where YMS tools allow scripting by customers, it is highly advantageous for the YMS administrator to learn the preferred scripting language (e.g., Perl, C++, Python) so that he or she can make minor data processing adjustments as needed without waiting for the YMS vendor to provide a fix.

Final Thought: The Conscientious YMS Administrator

Technical skills alone are of limited value unless combined with a perfectionistic approach to data integrity and robustness of the system on the part of the YMS administrator. A conscientious YMS

DR. ROAWEN CHEN
Vice President, Manufacturing Operations, Marvell Technology Group Ltd.

Marvell's continuous sequential revenue growth is due in part to the company's superior supply chain management. In my interview with Roawen Chen, vice president of manufacturing operations at Marvell, and member of GSA's board of directors, we discussed how Marvell delivers great efficiency, what value-adds the company provides to its customers, how mobile computing devices will revolutionize the industry and much more.

— Jodi Shelton, President, GSA

Q: *How has Marvell been able to produce operational efficiencies within its supply chain?*

A: Marvell runs one of the most efficient business operations in the industry. Over the last 12 months, we shipped more than one billion units of roughly 600 active products. In Q1 2010, our gross margin was 60 percent, and Marvell's on time delivery was close to a historical high while the inventory level was at a historical low. This means that although supply remains constrained, we believe we manage our supply chain very well.

Marvell has a small operations team, so how do we deliver this great efficiency? First, our industry has a fairly simple supply chain—a few foundries, a handful of packaging/testing houses and other suppliers. Since the founding of Marvell, we have formed strong partnerships with key supply chain vendors with the belief that the partnership must be long-term and reciprocal. The partnership cannot be transaction-based. Second, the past has proven that flexibility and agility are the most crucial elements of superior supply chain management, and Marvell deeply values both. Third, as a fabless semiconductor and an IC component company, Marvell optimizes its supply chain based on the assumption that its crystal ball used to forecast the market is obscure at best. This sounds pessimistic, but it is very true. As such, instead of only focusing on improving forecast quality, we put forth a large effort in hedging the risks of demand misforecast. With this in mind, our supply chain helps us deliver magic consistently.

Q: *Scott Grant, managing director of Accenture's semiconductor business, recently stated that companies must shift from transaction-based companies to value-valued companies to succeed. What value-add is Marvell planning to deliver to its customers?*

A: Marvell is definitely in the value-add business. Ten years ago, Marvell's value proposition was delivering differentiated intellectual property (IP) or functionality. Today, however, in addition to providing differentiated IP, we must be a complete solution provider. We also need to integrate more IP into a single chip which will, in turn, reduce the overall cost for our customers.

Q: *With a large consumer base in Asia, how much of the company's manufacturing is outsourced to foundries located in this region, and how does this benefit Marvell's product output?*

A: Marvell strives to work with the best foundries in the industry, regardless of their location. Foundry selection is independent of the geographic location of our customers. While our supply chain has a large concentration in Asia, our customer base is global and fairly evenly distributed throughout the world. We believe the biggest benefit is working with the best.

Q: *Have you seen an increase in the number of foundries offering leading-edge process technology? Does Marvell differentiate itself by process technology alone? Tell us about some of Marvell's leading-edge designs.*

A: Based on our observation and external analyst reports, fewer

foundry players can continuously afford leading edge technology due to financial and technical feasibility. Therefore, I have not seen an increase.

Since the beginning of the fabless industry, Marvell's focus has been on making the best products through design. Differentiating our products by process technology is of course important; however, as a design house, we put less focus on customizing our own process technology. Our leading-edge designs include a number of 28 nm test chips. These new products will serve the storage and mobile communications market.

Q: *As a newly elected member of GSA's board of directors, you will help shape the direction of the organization and contribute to solving industry challenges. From a manufacturing perspective, what are the on-going issues today that need the most attention from the industry?*

A: One issue the industry needs to address is how to keep pace with Moore's Law and beyond, which is becoming very challenging. Another industry issue is that a chip's manufacturing cycle time is becoming longer as process technology advances. In many cases, the manufacturing cycle time is longer than business visibility which creates many challenges in supply chain management.

Q: *The successful tablet market is grabbing significant share from the notebook/netbook market, creating major implications for the mobile supply chain according to Barclays analysts. As a company aimed at the mobile device market, do you believe the tablet will serve as an add-on*

25

As chip integration advances and costs increasingly rise in today's industry, the value chain producer (VCP) business model is proving to be a valuable asset to the supply chain, providing cost-effective solutions to these challenges. In my interview with Jack Harding, chairman, president and chief executive officer of the largest independent semiconductor VCP, eSilicon, and member of GSA's board of directors, we discussed how the company can potentially increase the profitability of the industry through its well-established relationships, where the value of the supply chain lies and much more.

— Jodi Shelton, President, GSA

JACK HARDING
Chairman, President & Chief Executive Officer, eSilicon Corporation

Q: *As a VCP, eSilicon's unique business model addresses the critical need for strategic collaboration within the semiconductor ecosystem. Define a VCP and how it can ease the difficulties fabless companies face early in the chip development process.*

A: A VCP company is a direct response to the disaggregation of the global semiconductor supply chain. We strive to re-aggregate the companies that have disintegrated. We combine both commercial interests and value-added engineering to create an one-stop shop for complex chip development. The resulting product has our customer's name on it, not ours.

We ease the burdens fabless companies face on several fronts. Commercially, we have aggregate buying power, which is enhanced by suppliers encouraging us to be a channel for them. We can find and eliminate financial inefficiencies within the ecosystem. Technologically, as chip complexity increases, having at least one organization in the supply chain with in-house engineering talents that can be shared across multiple companies and chips is essential. This keeps companies from having to hire a stable full of experts that would not need to be utilized on a full-time basis.

Q: *Who are some of eSilicon's partners, and what criteria does the company consider when developing its supply chain relationships?*

A: Over the last 10 years, the supply chain has undergone significant change which has required eSilicon to engage with virtually every company in the chain. However, our lead and most important supplier has been and continues to be Taiwan Semiconductor Manufacturing Company (TSMC).

In terms of selecting supply chain partners, more often than not, our customers approach us with a set of technical requirements that dictate a specific area of the supply chain and specific suppliers. But from time to time, customers ask us for advice when it concerns deep technology. For example, they might have trouble choosing intellectual property (IP) from 10 different suppliers. eSilicon has the expertise to advise customers on picking the most optimal IP solution within an acceptable budget. I would say 80 percent of the time eSilicon's partnerships are previously determined by the customer, and the remainder is spent recommending suppliers that will optimize the customer's chip.

Q: *Recognizing the vital role that the VCP business model plays in tackling the many challenges chip companies face today, GSA added a VCP position to its board of directors this year. As the first VCP representative on the board, you will represent the needs and concerns of the VCP market. What are some current needs and concerns?*

A: With VCPs being a relatively new concept in the industry, wide recognition of the importance of the business model of re-aggregating companies within the global supply chain is needed. VCPs need to take on a bigger role in industry policy and business issues, which is why it is important that VCPs are vocal in the direction of GSA. The VCP representative will be able to advocate for small semiconductor companies that have had little say on policy decisions. Many of eSilicon's customers are either very small companies or large original equipment

manufacturers (OEMs), neither of which have a very large voice at GSA. The roots of GSA are, in fact, small companies, but they have now grown into large companies, so we can't forget those small companies that are lagging behind.

Q: *With a rare wealth of experience that spans the entire semiconductor supply chain, where do you feel the main value of the supply chain lies as outsourcing becomes more prevalent?*

A: Clearly, every member of the semiconductor supply chain has a critical role to play, but I believe the epicenter of the supply chain today is the wafer foundry, as it manifests the development of both IP and electronic design automation (EDA).

The utilization of research and development (R&D) within a given wafer is going to continue to increase in complexity. Foundries such as TSMC and GlobalFoundries have spent millions of dollars developing process technology to serve various markets. However, as those processes become more complex, it will become more difficult for the average company to access all the bells and whistles that exist within the wafer to make the highest quality die. If a fabless company is going to make one chip, which may or may not go to market, the foundry can't spend the time necessary to train the fabless company to be successful. We recently heard from one wafer manufacturer that they cannot afford to help every company be successful at 40 nm or 28 nm. So as companies face greater complexities, someone has to aggregate the know-how to make it work, and that's what the VCP does. In this circumstance, engaging with a VCP allows a company to be directed, through our

Hardware Emulation Proven to Reduce the Cost of Bringing a Chip to Market

Lauro Rizzatti, General Manager, EVE-USA

While the semiconductor industry laments the cost of getting products to market and bemoans increasing design complexity, crafty design teams are finding ways to beat these seemingly impossible challenges with a host of creative solutions.

In some cases, these design teams are relying on embedded software and not hardware as a product differentiator. Others are looking to the electronic design automation (EDA) market for tools that can deliver a solid and defensible return on investment (ROI). And those EDA companies whose products can meet ROI performance measurements have a far better chance of success and long-term survival.

The semiconductor industry is known for having short product life cycles, all the while being nimble enough to address fast-moving markets. This fast pace consistently produces tangible results, but studies show that being even three months late in product delivery can cost more than a quarter of the potential revenue. Market share gained by being first to market may outweigh any premium paid for investing in the EDA tools needed to complete the project on time and within budget.

That's why these considerations of affordability and the use of the best available EDA technology must be balanced with a business model of restraint, but with a nod to new architectural ideas and competent development efforts. The increased focus on ROI has forced many companies to think more carefully about their yearly budgeting, and design teams need to weigh the ROI performance measurement accordingly. In general, the EDA industry has found that its tool sales are driven by ROI, affordability and good value. Semiconductor companies must be able to justify the purchase.

For example, hardware emulation, also known as hardware-assisted verification, is one EDA tool making a resurgence. While such tools have been around for more than two decades, they used to be housed in big boxes, were excessively expensive and never achieved speeds in excess of 1 MHz. Slow speed had prevented their deployment as platforms for embedded software validation. Further, the combination of slow speed and a high price tag limited their adoption by large corporations, and they were used mainly for hardware testing of large microprocessor and graphics chip designs.

Conversely, the latest generations of hardware emulators are implemented in small enclosures, saving space, power and infrastructure costs. Best of all, they cost a fraction of the big boxes and execute at several megahertz—exceedingly fast by any measure. They now are considered universal verification tools that can be used across the entire development cycle, from hardware verification to hardware/software integration and embedded software validation. They can be used to accelerate an existing logic simulation environment and to increase the total verification cycles prior to tapeout.

These tools can be cost effective, if implemented properly, and can handle design sizes of up to one-billion or more application-specific IC (ASIC) gates at high speeds. With a lower overall cost of ownership than prior generations, modern emulators can help a design team reduce the cost of bringing a chip to market and achieve the solid ROI they're looking for.

Figure 1. ROI Benefits of Hardware Emulation

Hardware emulators are universal verification tools that can be used across the entire development cycle, from hardware verification, hardware/software integration to embedded software validation for solid ROI.

Let's consider today's chip design reality. Testing hardware and software together on the actual chip is difficult, time consuming and expensive. If the design team hits a hardware bug, it needs to re-spin the silicon, a costly proposition both in terms of time and budget. If the team hits a software bug, the bug may cause a pricey delay in getting the product to market. Co-verification of hardware and software at an early stage with the aid of an emulation system and before silicon availability is a viable and increasingly popular strategy for these reasons.

The ever-popular workhorse logic simulation is an excellent choice for debugging register transfer-level (RTL) code, while electronic system-level (ESL) simulation is helpful in starting embedded software validation before silicon. However, neither can

Section 337 Investigations at the U.S. International Trade Commission: A Powerful Weapon Semiconductor Companies Can Use to Block the Importation of Unfair Imports

Gary M. Hnath, Partner, Mayer Brown LLP

Semiconductors have been at the heart of most technological progress in the last few decades. The semiconductor market is highly competitive and characterized by rapid technological change. Manufacturers of semiconductors and fabrication equipment seeking to protect their intellectual property (IP) and prevent competition from unfair imports have a powerful remedy at their disposal which many do not even know about—Section 337 investigations at the U.S. International Trade Commission (ITC).

Section 337 prevents unfair acts in the importation of articles into the United States. The ITC has the power to issue exclusion orders which are enforced by U.S. Customs and prevent unfair imports from entering the United States. Indeed, for reasons discussed below, Section 337 is ideally suited to provide fast and effective relief in cases involving semiconductors. This article will describe the types of cases that can be brought under the statute, the types of remedies available, how a Section 337 proceeding works, and the advantages of using Section 337 vs. other remedies to block unfair imports in cases involving semiconductors.

Types of Cases That Can Be Brought under Section 337

Section 337 of the Tariff Act of 1930 is a statute which prohibits unfair acts in the importation of articles into the United States. Section 337 proceedings take place before the U.S. ITC in Washington, D.C. As the following graph shows, the number of Section 337 complaints filed has more than doubled in the past five years and continues to rise rapidly.

Figure 1. Increase in Section 337 Complaints Filed
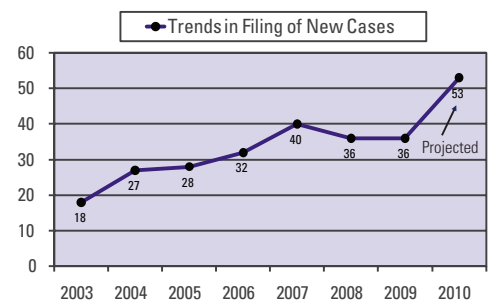
Source: Mayer Brown

There are three basic elements for showing a violation of Section 337 and getting an exclusion order from the ITC. First, it must be demonstrated that there is some unfair act involved. Second, there must be some connection between the unfair act and importation into the United States, or the sale of goods after importation. Third, a complainant must show that a "domestic industry" exists.

As to the first requirement, virtually any unfair act in the importation of articles can be asserted under Section 337. Over 90 percent of the cases at the ITC involve allegations of patent infringement. However, Section 337 complaints have been based on a variety of other unfair acts, including trademark and copyright infringement, trade dress infringement, grey market goods violations, unfair competition, trade secret misappropriation, passing off, and violation of the antitrust laws. The statute could be used for other unfair acts as well. For example, if products were being made abroad using factories that violate environmental laws, if illegal child labor was being used or if the imported products violated safety standards, Section 337 could provide a remedy.

While the ITC's jurisdiction is limited to cases involving imported products, this is not generally a difficult requirement to satisfy. As fewer and fewer products are actually manufactured in the United States, more and more products are made outside the U.S. and come within the ITC's jurisdiction. The importation requirement can be satisfied by any importation; a single sample imported for display at a trade show in the U.S. can suffice. A contract for sale may also satisfy the importation requirement even if no importation has yet taken place.

A company bringing a Section 337 case must demonstrate that a domestic industry exists. Once again, however, this is not usually a difficult requirement to satisfy. In a case involving "statutory" IP rights, such as patents, registered trademarks, copyrights and mask works, the domestic industry test can be satisfied through a variety of activities. Manufacturing in the United States is one way to satisfy the test but is not required. A company involved in significant or substantial activities relating to engineering, research and development, licensing, or even other activities such as quality control and after sales service may be able to satisfy the domestic industry requirement if sufficiently related to the IP right being asserted. Even foreign-based companies can also use the ITC to their advantage. Indeed, in 2009, over 25 percent of the complaints filed at the ITC were filed by foreign-based companies with U.S. operations.

In a case involving "non-statutory" IP or other unfair acts, such as trade secret appropriation, trade dress infringement, antitrust violations and so forth, a complainant must show injury to the domestic industry.

Injury can be shown, for example, by demonstrating that the unfair imports have been causing a loss of sales, lower prices or adversely affecting employment in the U.S. When actual injury has not yet occurred, the statute permits a showing of a "threat of injury." If a company is concerned enough to bring a Section 337 complaint, it is likely that it will be able to prove injury to a domestic industry under the statute.

How a Section 337 Investigation Works

The process at the ITC begins with the filing of a complaint by the complainant, outlining the alleged unfair import practices, the basis for importation and what constitutes the domestic industry. The Commission has 30 days to decide whether to institute an investigation. Typically, the Commission will institute as long as the complaint complies with the Commission's rules.

The case is then assigned to an administrative law judge (ALJ). The parties proceed much as in a typical court case, except that everything moves much faster. In general, parties will have 10 days to respond to discovery requests and motions, rather than 30 days or more as in most cases in federal or state court.

The parties in a Section 337 case exchange documents and other discovery and, where appropriate, submit expert reports. Any party can file a motion to resolve both procedural and substantive issues. The case then goes before the ALJ for a hearing or trial. Typically, trials at the ITC are in the range of one to two weeks. Any party can call witnesses and submit documents as evidence at the hearing.

After the hearing, the ALJ issues his decision, or initial determination, as to whether or not there has been a violation of the statute. Parties can ask the Commission to review all or part of the ALJ's decision. The Commission then issues its final determination on whether or not Section 337 has been violated, and if so, the appropriate remedy. A party adversely affected by the Commission's decision can file an appeal with the Federal Circuit Court of Appeals, but the ITC's exclusion order is in effect while the case is being appealed unless a respondent is able to obtain a stay of the order, which is unusual.

The Advantages of Using Section 337 in Semiconductor Cases

Section 337 is ideally suited to protect the IP rights of semiconductor companies.

For one, Section 337 is extremely fast. By statute, cases must be resolved expeditiously. Typically, target dates are set which require the entire investigation to be completed, from initial institution of the investigation until a final Commission decision, within 12 to 16 months. This means that the case is likely to go to trial in less than a year, much faster than most federal or state courts. This is particularly important in an industry such as semiconductors where technology changes rapidly. An injunction from a district court that takes several years before a case is resolved will be of little use if the technology in the meantime has become obsolete. Section 337 offers a quicker alternative than most district courts.

The unique remedies available at the ITC are particularly advantageous to semiconductor companies. If the complainant prevails, the ITC issues an exclusion order that is enforced by Customs and prevents the importation of the accused products at the border. Moreover, in a district court case, an injunction would be limited to the specific products at issue or other products not "colorably different" from those products. An ITC exclusion order, however, can cover all products made, imported or sold by the respondents that are infringing, not only the products found to infringe during the investigation. This is especially useful where specific products have a short life cycle, such as in the case of semiconductors.

In addition, in certain situations, a complainant may be able to obtain a general exclusion order that prohibits the importation of all infringing products, regardless of source. These remedies are not available through the courts.

All known companies can be named in a single investigation at the ITC, including companies that are manufacturing infringing products outside of the United States, importing the products into the United States and selling the product after importation. In a typical court case, it may be necessary to bring multiple cases in different states to satisfy jurisdictional requirements.

In a court case, it may take several months to serve respondents in some foreign countries, and the complaint and supporting documents may need to be translated. In contrast, the ITC serves the complaint on all proposed respondents by certified mail without the need for translations. Companies named as respondents in a Section 337 investigation must answer the complaint and comply with discovery requests, or a default can issue and

How Semiconductor Companies Are Helping Counterfeiters

Chris Jensen, Vice President, New Momentum

Getting a higher than usual return rate or increase in quality problems is all too often the way many semiconductor companies discover their products are being counterfeited. Unfortunately, by the time a company reacts to these issues, they've already lost revenues, profits and brand reputation. What's more, customer safety may be at risk from these defective electronics.

By taking a proactive approach, semiconductor companies can reduce the impact of this illegal activity on their company. The first step is to change the behaviors that are actually making it easier for counterfeiters. This article will discuss five areas where semiconductor companies are enabling counterfeiters, and will also provide examples of how some companies have been successful in changing these behaviors. These five areas are loss of engineering samples, chips and intellectual property (IP); lack of management support; lack of a dedicated brand protection team; not monitoring online sales; and not having a follow-up process for enforcement.

How Safe Are the Company's Engineering Samples, IP and Chips?

A number of factors have coalesced to create a business environment in which manufacturing counterfeit IP is not only lucrative, but also more attainable than ever before. Counterfeiters are becoming increasingly tech-savvy, and their ability to obtain more advanced manufacturing machinery and techniques has been one of the most crucial factors in fueling the production of illegal electronics.

Figure 1. Top Trading Partners

China Remains the Top Trading Partner for IPR Violations

FY 2009 seizures of IPR infringing products from China totaled $204.7M and accounted for 79% of the total domestic value for all IPR seizures.

- Hong Kong's $26.8M in seized value makes it the second most significant trading partner by domestic value for IPR seizures, and accounted for 10% of the total domestic value.

- India had the third highest domestic value at $3M, accounting for 1% of the total domestic value.

Source: U.S. Customs & Border Protection, U.S. Immigration & Customs Enforcement

Based on seizures of counterfeit goods, a large percentage of which are electronics, U.S. Customs and Border Protection reports that China and India are responsible for most IP Rights violations.

During the past decade, billions of dollars in foreign direct investment have flowed into a number of developing countries, such as China, leading to the proliferation of sophisticated manufacturing processes and capabilities to produce high-tech products. Counterfeit components have long been a problem in the electronics industry, but as of late, companies are finding themselves increasingly challenged with having to deal with counterfeit semiconductor components. Unfortunately, many semiconductor companies are inadvertently making it easier for counterfeiters. Lack of control over outsourced products partners is a key example. While outsourcing has numerous financial benefits, the downside is that it takes extra time and effort to ensure chip security. There are a few things that a semiconductor manufacturer can do that have now become essential to protect IP.

- Monitor contract manufacturers and distributors already in the supply chain. Too often, once a company becomes a partner, there is very little oversight. Perhaps security requirements were in the original agreement, but who's watching to ensure compliance? It's essential that a team, teams or individual in the company has ownership for ensuring that all security requirements in the original agreement are being met. And if a company is not in compliance, they need to be put on notice. Typically, once their partners know their activity is being monitored, security gets tighter and compliance stronger.

- Interview companies and investigate their background before allowing them to become contract manufacturers, licensees of the company's IP, resellers or distributors. This sounds like a no-brainer, but unfortunately, it's a step that gets very little attention—particularly when it comes to contract manufacturers or licensees. In addition to standard due diligence, it's important to talk with previous clients and specifically ask the question about security compliance. For example, one fabless company uses a brand protection solution with advanced online search technology to monitor potential licensees for what may be violations of other semiconductor company's products. Once they determine the licensee meets their standards and they sign an agreement with them, the monitoring does not stop. They continue monitoring the new licensee for potential violations that include unreported sales as well as counterfeit issues.

- Once a company has entered the supply chain, in addition to establishing strict contracts upfront, semiconductor manufacturers can minimize exposure by performing extensive auditing and maintaining close relationships. Personal relationships make a difference. Considering distances and time zones for global partners is an area that also gets neglected and makes it easier for counterfeiters. Regular e-mails, phone calls and personal visits, when possible, go a long way in keeping chips, engineering samples and IP safe.

Lack of Management Support

Upper management wants to know how counterfeit abatement affects their bottom line. Most supply chain executives know they've got a problem with counterfeits. They know it impacts the sales effort, bottom line, brand reputation and customer satisfaction. The end customer doesn't know their device isn't working properly because there's a counterfeit chip in it. And the chip customer (the device manufacturer) may decide to go elsewhere because they are getting too many returns. But the supply chain manager often has trouble getting the management support and resources needed to deal with the problem. So how can a supply chain manager prove to upper management that an anti-counterfeiting or brand protection program will improve their bottom line?

First, it's essential to find the magnitude of the problem. In the past, many companies have tried to handle this through manual or semi-automated searching of the Internet. It was a tedious, time-consuming and generally fruitless process. Considering the volume of unrelated data that was returned and the analysis that needed to be done, most supply chain managers didn't have the reports they needed to gain management support for the resources required. However, now there are brand protection solutions available that have advanced search capabilities. These solutions are capable of global monitoring the Internet, reaching sources in developing countries that would be difficult or impossible to access any other way. Additionally, the best of these solutions don't only bring back data, but are also capable of prioritizing data so potential counterfeiters are ranked from worst to least. In addition to the initial data showing the magnitude of the problem, this ranking helps demonstrate to upper management where the best and quickest return on investment (ROI) can be achieved.

Lack of a Dedicated Brand Protection Team

Even the most sophisticated electronics industry brand protection programs started out small and grew as they showed results. One company that has a brand protection group that has had extraordinary results, including $200 million plus seizures of counterfeit products by the U.S. Customs and Border Protection as well as significant reductions in counterfeit activity and quality problems started with one-and-a-half people on their team. Eight years later, they're a 40-person group that is incented on the amount of counterfeit activity they shut down. They report that they're saving the company billions of dollars every year and that their team has excellent ROI.

Without management support, often supply chain managers or quality team leaders are expected to add anti-counterfeiting to their portfolios. Not only is this difficult, but it also generally doesn't work. Someone needs to take ownership and have the clout to not only find the culprits, but also launch enforcement proceedings.

Here's an example that didn't work. One semiconductor manufacturer set up a virtual anti-counterfeiting team. The team leader and other team members all had other positions, and this portfolio was added. Everyone knew the company had a problem with counterfeits, but they were all busy people. When the team leader engaged a brand protection solution provider to monitor their products online, the first thing he needed to do was get a list of target engineering samples and chips, along with pricing, to the solution provider. After 10 months of trying, he was unable to even gather the data needed to get the process started. Meanwhile, he estimated that billions were being lost to counterfeits and potential business lost to lower customer satisfaction.

Not Monitoring Online Sales

E-commerce is a primary driver of the growing counterfeit market. Daily visibility into a broad variety of market intelligence data that can be used to identify suspect products and companies is essential. This visibility enables a proactive response to head off counterfeiting before it hurts a company's brand and bottom line.

Today's online monitoring solutions, which are based on advanced search technologies, offer 24/7 visibility into the global, open market. Without this extensive visibility, a semiconductor company's IP and products are at risk. Because counterfeiters go on the Internet, sell what they can and then go off in 48 hours, only to come back online again under a different name or Internet Protocol (IP) address, weekly or monthly searches can't find the most sophisticated counterfeiters—the ones who are weakening the bottom line the most.

It is also critical that a semiconductor company monitor the global market—particularly in developing countries in Asia and Eastern Europe. The advanced brand protection solutions should be able to monitor activity in these countries and translate the results as well as provide them in local languages. It's important when monitoring China, for example, to monitor both the English and Mandarin sites.

Figure 2. Potential Counterfeit Activity by Revenue Loss

Study | 1 Global Semiconductor Company from Jan 23 - Feb 18, 2008

Report on all products 50% or greater discount.
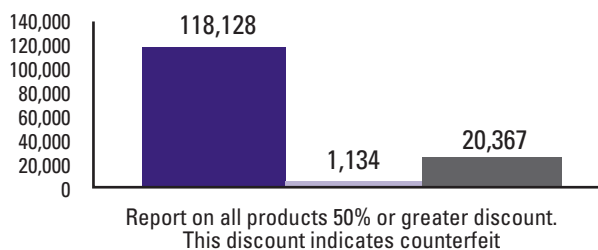This discount indicates counterfeit
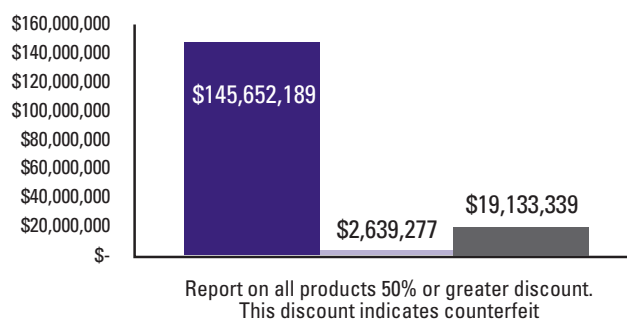
■ Counterfeit ■ Gray Market ■ Authorized Distributor

Here's an example of the value of counterfeit activity one semiconductor company found in less than 30 days using an online monitoring system. Typically, products offered on the Internet at a 50 percent or more discount are counterfeit.

Figure 3. Potential Counterfeit Activity by Quantity

Study | 1 Global Semiconductor Company from Jan 23 - Feb 18, 2008

Report on all products 50% or greater discount.
This discount indicates counterfeit

■ Counterfeit ■ Gray Market ■ Authorized Distributor

After tracking potential counterfeit activity for less than 30 days, the same semiconductor company found that the amount of counterfeit products on the open market far exceeded their original estimates.

Not Having a Follow-Up Process for Enforcement

Once the data is delivered via the brand protection solution, the anti-counterfeiting team needs to have the resources to start enforcement

Cost Realities in Bringing a Chip to Market

Sanjay Krishnan, Business Manager, High-performance Analog Group, Maxim Integrated Products

I n the semiconductor and electronics industries, chip costs are commonly thought to be dominated by manufacturing. One reason for this is the fact that it can take well over $1 billion in capital expenditure to set up a modern semiconductor fabrication plant. In addition, operating expenses are under constant watch by supply chain and operations executives. A good portion of research and development (R&D) investment goes towards bringing manufacturing costs down to boost margins. Finally, investors see good capacity utilization as an indicator of good management planning.

Operational Costs

Let's take a look at some of the chip development costs incurred by those companies whose brand is on the chip. EDA tool and foundry costs are expected to be accounted for in the development cost of the final product. Apart from manufacturing costs, bringing a chip to market involves several other operational activities such as R&D, marketing, sales, administration and overhead. All these activities influence the productivity and profitability of a company. A sample of large fabless companies and integrated device manufacturers (IDMs) and their quarterly earnings is shown in Table 1. As a revenue-weighted average, non-manufacturing operational costs account for 31 percent of revenues, while manufacturing costs account for 44 percent.

Table 1. Manufacturing and Non-manufacturing Costs in the Semiconductor Industry (2010)

Company	Revenue ($M/Q) (*)	Mfg Costs (**)	Other Operational Costs (**)
Intel Corporation	$10,299	37%	30%
Advanced Micro Devices	$1,574	53%	36%
Texas Instruments Inc.	$3,205	47%	23%
Broadcom Corporation	$1,462	48%	38%
STMicroelectronics N.V.	$2,325	63%	38%
ARM Holdings plc (ADR)	$134	8%	65%
NVIDIA Corporation	$1,002	54%	31%
MIPS Technologies, Inc.	$18	0%	77%
	Revenue-weighted Average	44%	31%

(*) Latest reported quarter.   *(**) As % of Revenue*

Manufacturing costs can come in at below 1 percent of revenues for companies that do not engage in actual production but derive their revenues from royalties. However, these costs will become part of the chip vendor's costs as they must pay these royalties. Looking at stable companies, whether they have adopted a fabless or IDM model, manufacturing costs converge towards 50 percent of revenues. Compared to the industries represented in major stock market indices, the semiconductor industry's manufacturing costs are fairly low. In fact, the pharmaceutical and bio-tech industries are quite similar to the semiconductor industry with their high gross margins and upfront product development costs.

A Three-stage Process

Bringing a chip to market can be roughly broken into three stages, taking a total of 1-3 years depending on the complexity of the product and the dynamics of the market. Let's again consider chip vendors here—foundry, test and assembly companies have a supporting role in this context since they do not sell the final product. And let's also focus on non-memory semiconductor products, as the financial story of the memory sector is different from the rest of the industry.

The first stage is planning, which includes marketing and R&D to justify the development of a particular technology or product. It's often a low investment area since it does not involve a significant staff or equipment commitment. Inadequate attention to this stage has led to many poorly defined products and projects being cancelled in practically every company in the industry. Some of the most important considerations to be made during this stage are profitability, risk and embedded options.

Profitability and risk are relatively well-understood terms, whereas the idea of embedded options is not formally considered in most companies. The term refers to hidden opportunities to address future markets that may be uncovered by investing today in the development of a certain technology. Some technologies or inventions are more fertile than others in allowing a diversity of future options, making them more attractive. The value of these options can be quantified in a rough manner to choose the most promising investment.

The second stage is chip design, which takes a good deal of R&D investment in the form of engineering hours and tools to support the design process. Often, software and hardware development must happen simultaneously for system testing and simulations to proceed successfully. Tapeout marks the end of the second stage. For digital processor or system-on-chip (SoC) companies, the investment here can be well into the tens of millions of dollars, while makers of small chips and analog chips can expect the investment to be around $1 million. In addition, there is the one-time cost to manufacture a photolithography mask set, which ranges from $0.1 million to over $1 million in finer geometry processes.

The third stage involves testing, validation, market acceptance and production. Performance and price determine the market acceptance of a chip. Manufacturing yield of defect-free products that are easily manufacture-able and testable determine profitability at this stage of the game.

On average, depending on the market, a commercially successful chip pays back the initial investment in 1–3 years after start of mass production. Keeping in mind that perhaps 20 percent of developed chips actually become successful, the average payback period is significantly longer.

Future Directions

Many of the fixed costs associated with chip development have been steadily rising. R&D involves larger teams working with increasingly sophisticated software tools which include more complex functions that are becoming more expensive to manufacture and test reliably.

With increasing product development costs, semiconductor companies will find it more difficult to contain R&D expenses. However, so far this has been offset by the manufacturing cost per unit decreasing with each successive technology node. In the long term, the focus will move towards generating a higher percentage of successful products. For this to happen, the chip design industry will need to focus on the productivity of non-manufacturing assets. These include R&D, marketing and sales which have a large bearing on the revenue-generating potential of semiconductor products. A successful product definition and marketing effort should drive margins substantially higher, providing funds for further investment and growth. It will also provide the higher multiples that CEOs look for in stock prices, as capital markets often evaluate equities based on a multiple of earnings.

There will continue to be a commoditized sector of the industry, including such capital-intensive sectors as memory. The dynamics of this sector will likely follow the expected boom and bust cycle. Silicon manufacturing, which has attracted competing capital investment from government and large private institutions in Asia, will not be highly profitable, but will enable chip design companies to thrive by lowering manufacturing costs and barriers to entry.

Cost containment efforts in these sectors have also led the industry towards very lean supply chains, resulting in periodic overcapacity and under-capacity. This volatility comes at a cost to investors since this sector and the industry itself has seen faster price erosion and more fire sales of underperforming assets and business units in recent years.

Conclusion

Bringing a chip to market has significant upfront costs (both manufacturing and non-manufacturing) that are recovered over the life of the product. These upfront investment costs are rising and are expected to continue increasing during the next decade. Emerging companies in the industry need to recognize the importance of product planning, design and marketing in bringing a chip to market successfully. The $1 trillion electronics industry served by the semiconductor industry is becoming increasingly specialized, and the semiconductor industry will evolve in the same way. Successful semiconductor companies will be those that align their investments with building relevant products and forming smart partnerships with customers to share knowledge and co-invest in the upfront costs. ∎

About the Author

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Alvand Technologies is a leading analog IC design house that specializes in high-speed, low-power and ultra-small die area data converters (i.e., analog-to-digital converter/digital-to-analog converter (ADC/DAC)) and analog front-ends (AFE) for a wide range of applications such as wireless (i.e., Wi-Fi, Worldwide Interoperability for Microwave Access (WiMAX), Long-Term Evolution (LTE)) and wireline (i.e., 10GBASE-T) communication systems, ultrasound and mobile TV. Alvand also provides full turnkey mixed-signal application-specific ICs (ASICs) based on the company's high-performance and low-power intellectual property (IP) cores. Alvand's analog and mixed-signal IC designers are industry veterans who have extensive experience in high-performance design with particular emphasis on ultra low-power applications.

ADC/DAC circuits become circuit bottlenecks and problem areas in semiconductor development because they are viewed as ancillary to the semiconductor's primary requirements. And due to time and cost pressures, a semiconductor's custom ADC/DAC circuit development and requirements tend to slide away from optimal performance levels. Alvand has spent 10 years narrowly focused on creating optimal ADC/DAC design flow algorithms so as to automate the design and insertion of ADC/DAC circuits for mixed-signal semiconductors. This design paradigm allows Alvand's customers to enjoy custom ADC/DAC circuits that are smaller, have fewer errors and greatly reduce development costs. ∎

"THE ART OF ANALOG DESIGN"

"Alvand Technologies joined GSA to increase industry awareness of Alvand's unique abilities and technologies, and through the alliance identify future business opportunities. GSA is a fixture in the fabless semiconductor community and Alvand looks forward to lending support to key industry initiatives."

– Mansour Keramat, Chief Executive Officer & Co-Founder, Alvand Technologies

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THIS SECTION IS DESIGNED TO ACQUAINT READERS
private showing
WITH GSA'S PRIVATE SEMICONDUCTOR MEMBERS

Parade Technologies, a 5-year-old fabless semiconductor company, is a leading supplier of high-speed digital display ICs. Parade's product portfolio includes highly integrated digital display and high-speed interface ICs that comply with DisplayPort, High-Definition Multimedia Interface (HDMI), Serial Advanced Technology Attachment (SATA) and Universal Serial Bus (USB) standards. Parade products are widely used in computers, consumer electronics and display panels.

Continuous advances in display resolution, color depth, refresh rates and 3-D performance require on-going innovation in digital display architecture and interface silicon capability. Parade leverages its close collaboration with market-building Tier-1 original equipment manufacturers (OEMs) and its active participation in standards-setting bodies to develop ICs that provide unique system capabilities, and which are optimized for system signal integrity and power efficiency. Parade is a key contributor to the Video Electronics Standards Association (VESA) DisplayPort standard.

As a result of the company's "standards-plus" design philosophy, Parade ICs have been designed into products sold by nearly every leading computer and display vendor worldwide. Founded by a group of experienced technologists and serial entrepreneurs, Parade is backed by strategic investors, including Intel Capital, United Microelectronics (UMC), Asia Vest Partners and Legend Capital. With a track record of rapid growth, Parade was chosen in 2009 as a finalist for GSA's annual Start-up to Watch award. The company is headquartered in San Jose, California. ∎

"Parade Technologies is firmly committed to supporting industry initiatives, whether it is working with VESA to develop the next-generation DisplayPort standard, or participating with GSA in information sharing and industry advocacy. We are proud to be active members of GSA."

– Jimmy Chiu, Vice President, Marketing, Parade Technologies

Jack Zhoa, President & CEO
Mark Qu, VP, Engineering
Ding Lu, VP, Product Development
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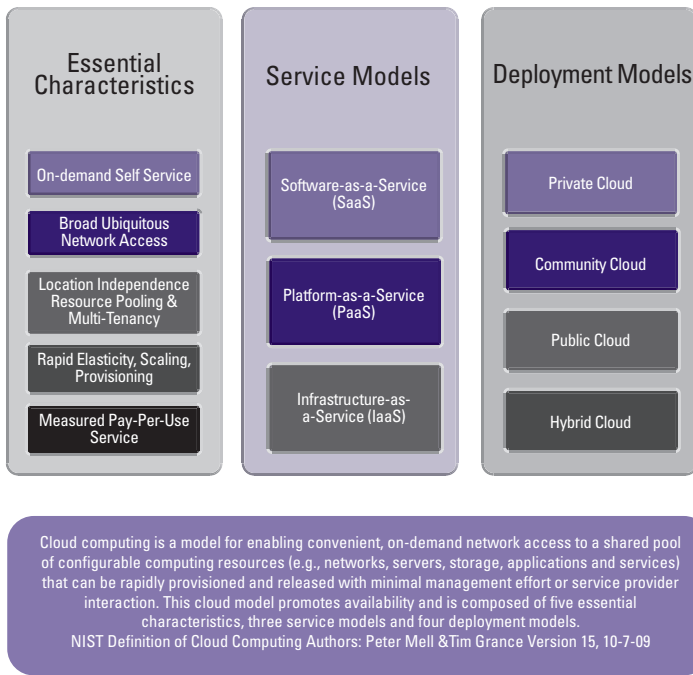
Camille Kokozaki, President, Design Rivers

In the early days of electricity and before power grids were available for business and home uses, generators were used locally by enterprises to create energy needed for the size or type of application or product offered. This created additional costs and logistics constraints that detracted from the business at hand. Then someone came up with the concept of pooling the needs of city blocks, followed by entire cities and finally regions, and delivering power to them by building enormous electricity generating plants that leveraged resources such that the net effect was a tremendous economy of scale, significant cost savings and an increase in productivity for all consumers of those resources. The concept of power grid and utility was born with a fixed-rate fee (adjusted periodically) that, when coupled with actual usage, set the variable operating cost of energy for the consumer.[1]

Fast forwarding in time and looking at a different industry and ecosystem, namely the semiconductor industry comprised of foundries, integrated device manufacturers (IDMs), and electronic design automation (EDA) and intellectual property (IP) providers, one finds a resource provisioning very much like in the early days of electricity. The ecosystem shows a fragmented supply and build-your-own tool procurement with complicated pricing and support structures—business models that sometimes inefficiently pile all-you-can-eat unneeded software on top of the few requested in exchange for a minimum size software order, which usually is a substantial amount of the committed tool budget. In other cases, one sees start-ups making do without needed tools, struggling to develop products with the smallest financial impact. The inefficiencies of developing potentially redundant tools; the struggle of software start-ups to compete with established vendors; the logistics of evaluating, procuring, deploying and supporting tools to develop end products; and the constant drive for EDA cost controls all contribute to sub-optimize the supply and the demand potential for EDA productivity tools.

Contributing to the emergence of the need for new transactional models is the fast evolution of information technology (IT) migrating from location-based, traditional server environments to virtualization of location leading up to full deployment in what is now identified as cloud computing. This is a dynamic, new paradigm that is seeing rapid shifts and includes many overlapping fields, unique definitions, interpretations, use cases and incarnations. The IT and software enterprise industries are attempting to put some formalism in the various definitions, and the U.S. National Institute of Standards and Technology (NIST) has weighed in on the definition of cloud computing. Figure 1 outlines the essential characteristics and the service and deployment models while providing a definition and classification. The driving forces behind cloud computing intend to provide optimizations to the capital and operational expenses in infrastructure resourcing by injecting efficiencies in deployment, maintenance and scaling to increased usage. The idea is to also improve user productivity and flexibility. In this definition, Infrastructure-as-a-Service (IaaS) provides the servers, storage and network for the user to provision/deploy operating systems and applications. Platform-as-a-Service (PaaS) is layered on top of the custom applications created and supported by the provider, and allows the user some control over the deployed applications and hosted environment configurations. Software-as-a-Service (SaaS) notches that up by providing a browser-driven thin-client connection to the whole environment being fully deployed in the cloud infrastructure, leaving only limited user-specific application configuration settings. The deployment types beyond the traditional private cloud (which most companies have been known to use) are (1) the community cloud shared by multiple organizations that have common needs or affinities, (2) the public cloud that provides access to the general public by a third-party organization that can support securely multiple tenants, and (3) the hybrid cloud which is a combination of any of the above but has standardized protocols, data and application portability, and a common taxonomy of procedures and methods. This last hybrid cloud is where the opportunity lies for the semiconductor/EDA/IP ecosystem.
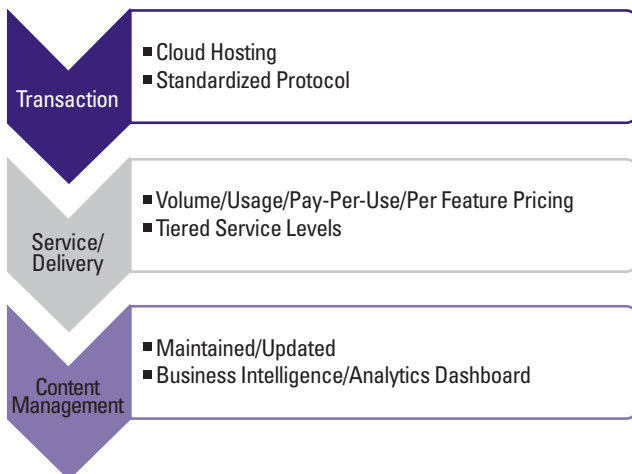
Figure 1. NIST Definition of Cloud Computing

Essential Characteristics	Service Models	Deployment Models
On-demand Self Service	Software-as-a-Service (SaaS)	Private Cloud
Broad Ubiquitous Network Access	Platform-as-a-Service (PaaS)	Community Cloud
Location Independence Resource Pooling & Multi-Tenancy	Infrastructure-as-a-Service (IaaS)	Public Cloud
Rapid Elasticity, Scaling, Provisioning		Hybrid Cloud
Measured Pay-Per-Use Service		

Cloud computing is a model for enabling convenient, on-demand network access to a shared pool of configurable computing resources (e.g., networks, servers, storage, applications and services) that can be rapidly provisioned and released with minimal management effort or service provider interaction. This cloud model promotes availability and is composed of five essential characteristics, three service models and four deployment models.
NIST Definition of Cloud Computing Authors: Peter Mell &Tim Grance Version 15, 10-7-09

The proposition here (Figure 2) is to lay a blueprint for improved EDA/IP synergies with the semiconductor user through the creation of support layers for:

- Transacting via a cloud-hosted standardized protocol sharing common taxonomy and procedures.

- Service and delivery with tiered service levels and volume usage/pay-per-use/per feature.

- Content management through maintained and updated analytics dashboards, standardized usage and activity reports.

Figure 2. Fully Leasable On-demand Engineering Utility Resourcing (FLOEUR) Support Layers

Transaction
- Cloud Hosting
- Standardized Protocol

Service/Delivery
- Volume/Usage/Pay-Per-Use/Per Feature Pricing
- Tiered Service Levels

Content Management
- Maintained/Updated
- Business Intelligence/Analytics Dashboard

If one takes a radical approach at re-architecting the entire semiconductor ecosystem with a different business model that changes the format of the supply and custom tailors usage by pay-per-use and all-you-do-need tools, this radical approach would look like the following:

- A flat rate usage fee per user, plan or type of tool.

- Year-over-year rate discounts based on any exceeded target usage volume for some of the tools.

- All EDA tools and IP offerings are bundled through a unified clearinghouse. IT and server access can also be optionally bundled into a full turnkey provisioning with everything delivered through one access point to multiple products from disparate vendors.

- Any existing contracts get transferred in terms of remaining monetary value and get depleted at the established yearly rate year-over-year if a lease model was in place or a permanent license re-buy credit occurs if tools were bought instead of leased.

- There is no concept of local area network (LAN)/wide area network (WAN)/maintenance support. One gets instant-on access.

- IP tools get exercised through the flat fee model (for verifying the IP), and the actual IP usage calls for a manufacturing usage fee per chip that can allow unlimited instances on-chip. This last portion could also be administered by the foundry.

- The flat rate fee will reflect actual usage by the user community and will not be some arbitrary number set to meet some desired margin, nor will it be influenced by an arbitrary discount solely set by quarter-end driven deal making. Warming up to even the concept of this transacting model could be challenging to the traditional way of selling in this ecosystem. On the other hand, many are questioning the viability of never-ending price wars, making it difficult to make any profit if users are complaining about expensive tool costs. Something is wrong when no one is happy in this transacting process.

- Customers will be able to have predictable computer-aided design (CAD) budgets that are optimized for usage through a timely review of tool usage based on projected internal demand. Customers will be able to have real-time usage tracking abilities.

- The playing field will be leveled for suppliers and customers alike in the sense that EDA start-ups and small-sized companies will be able to compete with their respective bigger competitors.

- Key metrics can be culled from usage patterns as it will become easier to quantify actual demand for design and manufacturing, allowing for increased investments in popular, needed products and features.

Flat rate fee tiered structures and options can be as follows:

- Flat corporate fee per month or quarter.

- Flat site fee per month or quarter.

- Flat rate pay-per-use fee per month or quarter.

  - Cost=Σ(monthly/quarterly module or feature rate)x(actual module or feature usage).

The key item to note here is that all EDA tools from separate vendors are being bundled as a package, enormously simplifying the administration and maintenance of the design environment on the supply and the demand side. The default settings would always have the latest released version from every supplier with the option to revert to any version a user requires.

The enabling of so many features with such a sweeping business model may raise concerns or objections: Will this bring down the growth, profitability and desirability of the EDA and IP space by

The Future of Mobile Electronics Interconnectivity

Hezi Saar, Senior Manager, SiPro Advanced Interface IP Product Line, Virage Logic

Mobile electronics is one of the hottest markets showing resilience despite challenging conditions. Today's mobile electronics market enters an explosive new era fueled by several trends and the introduction of new product categories. The hype around inexpensive netbooks, the introduction of pads and multimedia tablets, and the increased popularity of e-books triggered a new class of mobile user experience that will change consumption in many market segments.

The maturity of cellular and wireless technologies is the driving force behind the extremely high cellular phone adoption rate in a number of countries, and it continues to spread ubiquitously around the world. The increased adoption of smartphone usage, coupled with data-intensive network coverage, enabled the widespread dissemination of content and value-added services.

The need for higher bandwidth for mobile devices enabled by Long-Term Evolution (LTE) technology is driven by the increased consumption and generation of streaming video content captured by high-resolution cameras, faster access to memory storage, and faster downloads from the Web transmitted or displayed on single, multiple or split displays. These requirements are driving the adoption of high-speed (HS) interfaces for faster downloads, storage access, and transmission of data and multimedia wirelessly or over wires.

Competitive Market Pressures

In today's hyper-competitive markets, being first to market with the right products is a critical element in business success. It's as important as ensuring the features selected and implemented are those needed, and that the cost of getting to market on time and with the right product features is achieved with minimal cost.

Tastes and technology change rapidly, making these challenges difficult to achieve. And management as well as engineers need to employ risk management techniques to mitigate technological and market pitfalls. Furthermore, verification costs have surpassed development costs, and the gap continues to broaden even with skyrocketing technology development and wafer costs.

In the mobile electronics market, mid- and low-tier mobile phones are already extremely cost-sensitive. The popularity of smartphones and new mobile electronics categories, coupled with a focus on value-added content, will make the high-end mobile market cost-sensitive and highly competitive on features and capabilities. Smartphones and netbooks, for example, approach the media tablet category from different ends which creates further uncertainties on competitive edge and differentiation.

Hence, to increase market share or simply stay in the game, mobile electronics original equipment manufacturers (OEMs) need to respond effectively to increasing competitive market conditions. Staying on top of the innovation curve requires design teams to focus on designing new features and upgrading platforms to satisfy changing tastes. Feature differentiation and rapid market introduction and deployment are essential for successful market penetration, and keeping the cost down is essential for increased profitability.

Smartphone Standardization

Making the smartphone a representative of the mobile device market, the smartphone looks more and more like a miniaturized version of a personal computer. The device has multiple capabilities, interfaces and components such as a storage card; one or more cameras for video and still capture; single, multiple and split displays; a cellular transceiver; wireless communication; power management devices; a speaker; and a microphone.

As reported by Generator research (2010), smartphones accounted for 13.8 percent of worldwide handset shipments in 2009, and will grow to account for nearly 25 percent by the end of 2014 when annual smartphone shipments will hit 371 million, which is over triple the annual growth rate of ordinary handset shipments during the same period.

It is important to note that major players (e.g., Google, Apple and Intel) are investing heavily in electronics and semiconductors for mobile markets because they are the next battle field in electronics technology innovation. Smartphones and mobile computing platforms allow for the delivery of value-added content anywhere, anytime as evidenced by the increased rate of applications downloaded, exceeding one billion per quarter[1]. The increased bandwidth driven by operators deploying wireless technologies (e.g., Third Generation (3G), LTE, Worldwide Interoperability for Microwave Access (WiMAX)) allows for the delivery of content that

was only available in broadband communications. The next frontier extends well beyond smartphones. Mobile electronics applications such as mobile computers for the business and home, mini notebooks, media tablets and e-books are all becoming key growth drivers for electronics and semiconductor use as they rely heavily on the latest wireless technologies and value-added content.

To address broad market requirements, mobile electronics OEMs will ideally use peripheral hardware products from multiple vendors that interface seamlessly with systems-on-chip (SoCs) and processors from different vendors to realize complete system functionality.

Chip-to-chip interface standardization for all inter-function connectivity in the mobile electronics environment enables compatibility, interoperability, integration, easily upgradable features, reduced pin count, increased system reliability, scalability, ease of test and debug, and potentially reduced power and electromagnetic interference (EMI).

For example, major handset OEMs use SoCs from different companies to meet different radio standard requirements. Since these SoCs come from different vendors, they vary in feature set, performance and interfaces to peripherals such as display and camera. Therefore, OEMs need to find display and camera modules that match the interface and capabilities of the SoC chosen for each platform.

The benefit of chip-to-chip standardization is clear from the design, technical, manufacturability and, especially, cost perspective as it is expected that standard-based ICs will ship in higher volume and allow for a cost reduction of the entire system.

Traditional camera and display interfaces utilize a parallel, high pin count link and, in some cases, low-voltage differential signaling (LVDS) to minimize pin count. Advances in camera and display resolutions and storage throughput is demanding that processors achieve increasingly higher performance with rich feature sets that result in exponentially higher power consumption. The power and performance specifications of parallel buses have made achieving economical and power friendly implementation difficult for many advance interfaces.

Increased performance/throughput while lowering overall power consumption helped to drive multi-core implementation and, in a similar way, helped transition from parallel interfaces to a serial solution.

Serial interface design is complex, but allows companies to achieve high performance, architecture scalability and successfully meet design targets such as reduced overall power consumption and EMI emission.

Figure 1. SerDes PHY Block Diagram Example
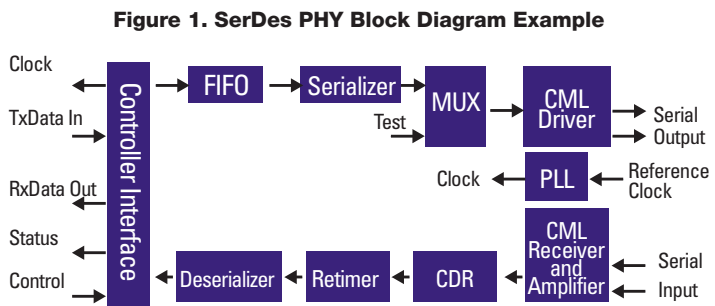
A serializer/deserializer (SerDes) implementation better meets a power budget than a parallel interface. The latter implementation employs multiple wires switching simultaneously, consumes more overall power (power per MB), complicates board design and adds signal integrity complexity (due to simultaneously switching signals).

The most notable chip-to-chip serial interface standards in the mobile industry are Mobile Display Digital Interface (MDDI) and Mobile Industry Processor Interface (MIPI). Both MDDI and MIPI specifications came about to eliminate the proprietary interfaces and reliability concerns of cellular phone designs and employ serial interface for low power (LP) and high throughput. Handsets featuring MDDI have entered the market in recent years; however, this standard didn't ramp-up as expected and received some adoption mostly in display applications.

By contrast, MIPI interfaces are getting significantly more market traction as major players in the mobile electronics industry are supporting and driving adoption throughout the entire value chain, thus creating a comprehensive ecosystem of solutions in all levels of design, test, verification, etc.

Mobile Industry Specifications

The MIPI Alliance is comprised of a family of specifications that have been developed over the past few years. The MIPI Alliance defines not just a single interface specification, but a collection of specifications aiming at the entire mobile device market.

Today, the path to MIPI adoption is clear for mainstream interfaces such as display and camera interfaces. MIPI interfaces have reached a maturity level on the SerDes-based D-PHY specifications as well as on the camera serial interface (CSI) and the display serial interface (DSI), as these are the most popular interfaces in mobile electronics. Today, they have become de-facto standards for mobile semiconductor devices.

The question is how a semiconductor device can quickly support these standards, especially when high-throughput, LP SerDes (e.g., MIPI D-PHY) is not their core competency. Companies that belong to the MIPI Alliance have created an ecosystem to help with adopting these interfaces. Providing proven intellectual property (IP) that covers the MIPI D-PHY and camera and display controller interfaces on common processes allows for easy, rapid and low-risk implementation. Thus, semiconductor vendors can quickly adopt MIPI and capture market share easily and effectively.

D-PHY, DSI and CSI-2

D-PHY is a physical layer implementation that provides a source-synchronous point-to-point connection between master and slave (or host and device) for other MIPI protocols (e.g., CSI and DSI). A typical configuration consists of a clock lane and one to four data lanes. The master/host is primarily the source of data, and the slave/device is usually the sink of data. D-PHY lanes can be configured for uni- and bi-directional lane operation, originating at the master and terminating at the slave. The D-PHY link supports a HS mode for fast data traffic and a LP mode mainly for control transactions. In HS mode, the low-swing differential signal is able to support data transfers from 80 Mbps to 1 Gbps. In LP mode, all wires operate as a single-ended line capable of supporting 10 Mbps asynchronous data communications. The D-PHY core can implement the PHY protocol interface (PPI) to easily interface to the required protocols (e.g., DSI and CSI-2 controllers).

Cliff Hirsch, Publisher, Semiconductor Times

An inside look at innovative semiconductor start-ups

The challenges for emerging semiconductor companies have never been greater. Yes, we all like the concept of a start-up hitting the ball out of the park, quickly capturing that billion dollar opportunity. But we all know that is rarely the case these days. Capital has become increasingly scarce while the cost of entry has continued to increase. That's why I like small, capital-efficient semiconductor start-ups that grow organically and patiently. These companies tend to exist in the low gate count analog and radio frequency (RF) world. **VectraWave** is a prime example.

VectraWave was founded in May 2006 to develop RFICs and system-in-package (SiP) devices for optical and microwave communication equipment providers. The company has raised a scant 1.2 million euros and has modest capital requirements going forward compared to capital-intensive digital system-on-chip (SoC) companies.

VectraWave is focused on direct current (DC) to millimeter-wave single functions and highly integrated semiconductors and application-specific ICs (ASICs), SiP modules and multi-chip modules (MCM) for microwave, RF and lightwave applications. In addition to custom products, VectraWave is developing off-the-shelf components and subsystems for the communications (hi-speed optical, broadband wireless and satellite), point-to-point and point-to-multipoint radios, aerospace and defense (radar and electronic countermeasures (ECM)), and broadband test equipment applications.

Current products include a variety of monolithic microwave ICs (MMICs) (DC to 100 GB), including coders, phase shifter drivers, drivers and amplifiers. VectraWave is developing a family of products, including 43 Gbps logic ICs with a sub-family of 43 Gbps coders, and has demonstrated a non-return-to-zero (NRZ) to return-to-zero differential phase-shift keying (RZ-DPSK) coder operating up to 43 Gbps in less than 1 mm^2 area.

VectraWave's first 40 GB coder circuit uses TowerJazz's 0.18 μm SiGe BiCMOS process instead of Indium Phosphide (InP), the traditional semiconductor material used for 40 GB circuits. The SiGe process enables digital circuits to be integrated on the same die, resulting in lower cost, lower power consumption, better temperature compensation and smaller total board area than equivalent InP-based functionality.

Roughly 80 percent of Vectrawave's products are custom; however, the goal is to move to a 50/50 mix of custom and standard products within the next several years. The company is focused on two key markets: 1) ICs and SiP for 10 GB to 100 GB optical communication equipment, which is estimated to be valued at $500 million within three to four years and 2) high-power amplifier (HPA) MMICs for microwave communication equipment, which is also estimated to be valued at $500 million within three to four years.

Competitors include TriQuint Semiconductor, GigOptix, Inphi, Centellax, Hittite Microwave, Mimix Broadband, UMS and several others. VectraWave believes its competitive advantages include comprehensive technology, highly skilled designers, European heritage and a focus on easy-to-use integrated devices. Notable customers include Alcatel-Lucent and Thales. ∎

Yan Haentjens, Co-founder & President
Alain Le Borgne, Ph.D., Co-founder; VP, Technologies
Hervé Cam, Ph.D., Co-founder & CTO
Gerald Chretien, Co-founder & Operations Director
Abdenour Chelouah, Ph.D., Co-founder & Engineering Manager
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their products can be automatically excluded from the United States.

Many semiconductor cases involve process patents. A Section 337 litigant can request an inspection of a foreign manufacturing plant to verify the actual process being used. While similar procedures are available in district court, requests for inspections may be met with long delays and may not even be possible if the manufacturer is outside the district court's jurisdiction. At the ITC, however, the manufacturer can be named as a respondent, and if it refuses to allow an inspection or provide an adequate inspection, its products may be excluded on that basis.

Furthermore, the ALJs at the ITC are very familiar with handling patent cases, and so a company will know it will be before a judge that is knowledgeable in these types of matters.

These are some of the reasons why the ITC is often the forum of choice for semiconductor companies asserting violations of IP rights and other unfair acts involving imported products.

Conclusion

As this discussion indicates, Section 337 can be a powerful remedy for semiconductor companies to prevent unfair competition from competitors that may be quicker and more effective than federal court litigation. At a minimum, semiconductor companies should weigh the pros and cons of a Section 337 investigation when considering their options to protect their IP rights. ∎

About the Author

Gary Hnath is a partner in Mayer Brown's Washington D.C. office. His practice focuses on IP litigation and counseling, including disputes involving patent, trademark and copyright infringement and trade secrets. He is a leading authority in the area of Section 337 litigation and former president of the ITC Trial Lawyers Association. Gary can be reached at ghnath@mayerbrown.com or 202-263-3040.

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commoditizing, in a way, all the distinguishing features of the tools and IP? The counterintuitive outcome could, in fact, re-energize and revitalize these two segments by unleashing an untapped source of revenue caused by users who may have shied away from using what they really wanted to use if they could afford it, or even simply manage their access to this new resource without significant effort.

The assumption here is that the applications can still run using the local infrastructure (private cloud), but there is nothing to prevent the bundling of even the servers as part of a full turnkey experience where the service, tools, server and storage are aggregated as a one-stop utility through a SaaS deployment. This would truly be like plugging in the appliance and worrying only about the design aspects and not the infrastructure or tool. The base service model is characterized as SaaS and what one can extrapolate to as IaaS if one wants full flexibility in managing the deployment. If one wants to manage the application development then one can graduate to a PaaS (Figure 3).

Figure 3. FLOEUR Model
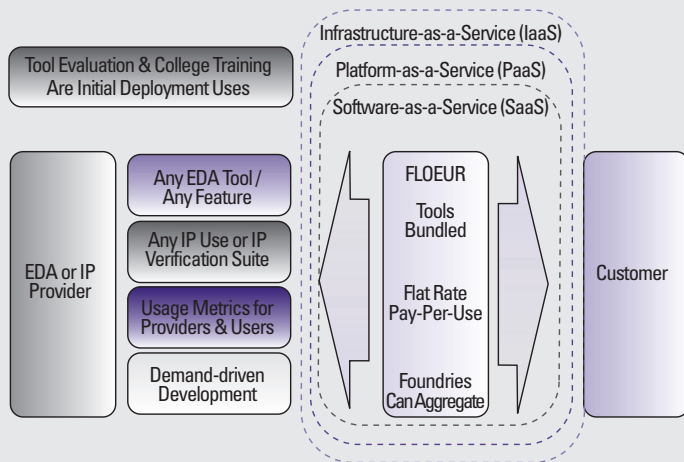
Pricing for the various features needs to be carefully calibrated to optimize use/value received from the tool capability and productivity enablement. The recommended next step is to pull together a committee representing the EDA, IP, IDM and foundry industries along with academia and industry associations, such as GSA or

Accellera, and to carefully review the mechanisms needed to bring about this transacting model. The IT and business analytics enterprise industries already have the necessary applications and infrastructure to implement and provision deployment in a cost-effective way. One can think of this as expanding the user space by increasing demand unfettered by an expensive access fee that slows down the velocity of development. What would be changing is the vendor-customer relationship, whereby the EDA industry works with larger providers, and customers have expanded access to all the available tool and IP space through a mega-channel with micro-access to a plethora of tools and resources. The idea of selling the tools would move from the obsession of closing the elusive large deal to better understanding what tool/IP solutions the customers are really after and feeding back improved feature requirements to the development team. Finally, there is no restriction in having only a select number of FLOEUR providers. Initially, these services could be offered and bundled by additional aggregators, including the foundries themselves who could bundle this along with their manufacturing services into a one-stop design service/tool/IP/silicon provisioning. If this leads to foundries acquiring EDA or IP as part of the vertical integration, all this would do is take the industry back to how it actually started with an all-in-one technology offering. Wouldn't it be nice to restart the rate of growth this ecosystem used to depend on? ∎

About the Author

Camille Kokozaki is president of Design Rivers. He most recently was with IDT as director of design automation services. During his 29 years of technology experience, Camille has held various management and engineering positions at Mostek and VLSI, including director of technology center operations. He was director of marketing at Philips Semiconductors and president of his own design services company. Camille holds a B.S.E.E. and M.S.E.E. from the University of Illinois at Urbana-Champaign and an MBA from Florida Atlantic University in Boca Raton, Florida. You can reach Camille Kokozaki at camille@designrivers. com or 408-705-7412.

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Management Priorities: The Supply Chain Executive Agenda

With these findings in mind, semiconductors companies and OEMs alike need to act on five priorities to ensure their supply chains are prepared for what lies ahead.

Priority 1: Improve Customer Collaboration and Accuracy in Supply Chain Planning

Companies have a variety of methods for responding effectively to volatility and its ripple effect throughout the supply chain. These include the use of point-of-sale data for forecasting (for OEMs), collaboration with customers and suppliers, and the use of real-time demand and supply planning.

Priority 2: Increase Upstream and Downstream Supply Chain Flexibility

The increased globalization and product complexities cited earlier will continue to test the supply chain agility of semiconductor companies and their partners. Supply chain executives need to have a number of potential solutions available, such as global footprint optimization, use of temporary resources and late-stage customization.

Priority 3: Focus on Total Supply Chain Cost Engineering

Supply chain organizations will continue to be viewed as a source of cost savings. Semiconductor and OEM executives can deliver on this promise by ensuring the right mix of outsourced and in-sourced operations, by developing regionally configured and optimized supply chains, and taking a "total cost" approach that considers often-overlooked process and management costs.

Priority 4: Implement End-to-End Supply Chain Risk Management

Top companies take a broad view of risk management. Following their lead, other companies need to step back and determine where there are the greatest risks of higher costs, increased working capital, and missed deliveries or service. It is important to look beyond the supply base and consider other sources of risk—everything from cash management to new product introductions, quality and safety.

Priority 5: Integrate and Empower the Supply Chain Organization

The ability to meet future challenges demands strong organizational capabilities. In particular, it requires efficient and effective collaboration within the organization and with partners, efficient decision making, and the right structure and talent. Semiconductor companies' supply chain executives should step back, make a broad assessment of their organizations' effectiveness, and implement changes that are necessary to develop their supply chain organizations to their fullest potential.

Semiconductor executives cannot afford to wait to prepare their supply chains for new market demands. They need to think beyond today's immediate challenges and consider how to manage costs while also effectively serving an ever-changing, global customer base. To capture benefits tomorrow, semiconductor companies need to act today. ∎

About the Author

Jim Takach, a director at global management consultancy PRTM, is based in the firm's Newport Beach office. Jim is a member of the firm's semiconductor and electronics business. His supply chain experience includes network optimization and outsourcing, site transition, warehousing and distribution, inventory management and supply chain benchmarking/assessment. Jim was also a member of the PRTM team that developed the Supply Chain Operations Reference (SCOR) model. He can be reached at jtakach@prtm.com or 949-255-5466.

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[1] www.PRTM.com/SCTrendsReport2010

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device for consumers, or will it be a strong competitor by itself in the PC industry? How do you see the mobile landscape evolving in the next few years?

A: The tablet market will obviously be a strong competitor by itself in the PC industry. In fact, our prediction is that it will reshape the roadmap of the future PC market.

Five to 10 years from now, mobile computing devices such as smartphones and tablets will become the largest segment in our industry's playbook. As the combined revenue for the PC and cell phone markets slows down, the smartphone and tablet markets will be the most promising segments that can generate enough revenue and profit to support next-generation research and development (R&D) of design and silicon process technology. We strongly believe this is one of only a few segments that can create sufficient value to sustain Moore's Law and beyond.

Q: *The wireless supply chain projected 3G technology to be its primary growth opportunity this year. However, cell phone baseband sales in Q1 2010 showed that companies (e.g., Marvell) focused on 2.5G technology were the top performers due to strong consumer demand in Asia. Is Marvell's focus on supporting older or newer technology?*

A: Marvell's business philosophy is that we provide products that add value for our customers; therefore, we focus on 3G technology as opposed to 2G. 3G accounts for more than 80 percent of our mobile phone business today. Roughly 99 percent of Marvell's R&D investment is in 3G and beyond.

Q: *Marvell has won multiple awards this year which highlights the company's reputation as a leader in innovation. Which aspect of the semiconductor supply chain do you feel is most important in sustaining innovation and creating new ideas?*

A: Marvell's key belief for supply chain management, as previously mentioned, is to treat those within our supply chain as valued partners rather than transaction-based vendors. By doing this, greater collaboration will naturally occur, which will lead to innovation. This is mutually beneficial to the success of Marvell and our suppliers and customers. ∎

are effectively flying blind, with only high-level "rear view mirror" metrics of development results. This can be too little, too late if they happen to get off track.

Leading companies address this challenge by adopting consistent, workable models for financial analysis of multi-tiered development, even if they're not perfect for every use case. The key elements of these models include:

- Thorough capture of development spend at both the individual project and at the platform/core IP levels.

- An allocation mechanism for distributing cross-project spend, such as core IP.

- Consistent models for product cost, including target cost analysis.

- Steadily maintained market and average selling price (ASP) models.

- A development proposal/project ranking based on gross margin or contribution margin metrics.

- A NPV-based "hurdle rate" total return benchmark for company financial performance.

Requirements Management

Requirements management offers two avenues to enhancing RoD. The first is associated with value engineering and design-for-cost disciplines, which force emphasis on feature-cost tradeoffs. It also counters an unfortunate tendency to "load up" product requirements unless they meet stringent criteria.

The second avenue is associated with time. A well-managed requirements process is time-sensitive, and requirements definition is notorious for being one of the most frequently extended stages of product development. Some companies even have "redefinition" as a named stage in their development process. Sure, you can argue that it's a fact of life, but extended development timelines create their own "redefinition" issues as the market passes them by.

The impact of time reduction on development financial performance is twofold. First, it reduces the uncertainty and the likelihood of changes to initial estimates. Second, time compression improves the NPV comparison of margin inflows and development spend.

Lean Engineering and Engineering Efficiency Management

A key driver for many companies is simply how much time each engineer or designer is actually able to devote to core, value-added tasks instead of administration, cross checking, error correction or sorting through disorganized information. Study this data and you will come away surprised by how high a percentage of your development staff time is unavailable for work that actually moves the process forward. By using value stream analysis and other lean techniques, a lot of engineers' non-productive time can be harvested and repurposed.

And let's be clear. Higher effective utilization of key technical resources is not only a cost reduction benefit. Again, it is a key lever for elapsed time. Now, the same staff can execute a given development effort in substantially less time than previously required and slash time-to-market.

Stage-gate Controls and Go/No-go Deployment of Development Resources

Many companies have established functioning stage-gate processes

that fairly clearly delineate the progress from requirements to design, first silicon and revenue launch. Yet far fewer incorporate the basic question, "Is it still worth it?"

The criteria that may have launched a development effort are often not revisited for a hard-headed look at whether they still hold water. In the quarters and years that elapse from initial development decisions to later gates, forecast prices may have eroded, estimated product unit costs may have risen, the cost to develop may have overrun and the realistic time-to-market may have elongated. Whether for good reasons or due to imperfect execution, all of these factors can change the original equation of the development effort's fundamental merits. In short, the potential for those hoped-for large returns may have evaporated.

Figure 3. RoD Leverage is Front-loaded in the Development Cycle
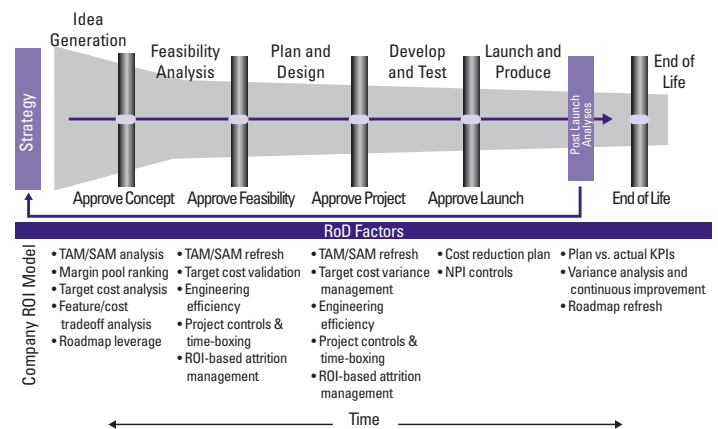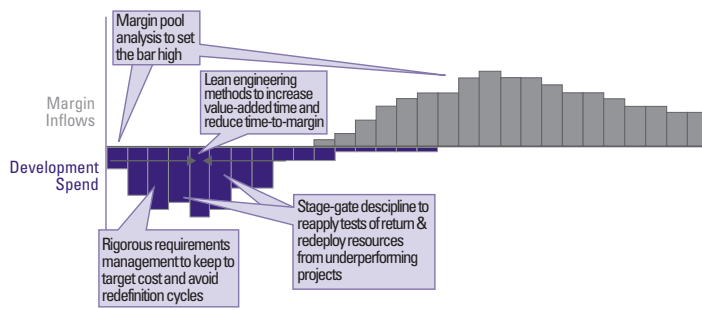

Source: Deloitte Consulting LLP

Any high-performing company will charter development projects that, for a variety of reasons, run out of runway before they make it to revenue ship. Here's a simple diagnostic question for your development process: "Do you ever kill projects?" If you can't answer yes, it's possible you are failing to identify and terminate unrewarding development efforts as early as possible in the process. And that means you may also be failing to recoup the available development resources and spend of a lackluster project that could be redeployed to more promising efforts.

Targeting Increased RoD

These are the basics, but implementing improvements that move the RoD needle have to come from all sides:

- Work on the right things. Apply useful financial tests to your portfolio before committing the spend.

- Work effectively. Implement lean-based engineering methods that increase the value-added component of your workforce's time. Stress test requirements to ensure that incremental value mitigates RoD impact.

- Continue to test ongoing projects against criteria for success. Be willing to terminate projects whose value proposition has faded, and re-invest teams' time into higher return efforts.

- Recognize the capital value of time reduction and the true cost of time spent redoing or reworking. Be willing to penalize the business case of laggard projects appropriately.

Figure 4. Accelerating Gross Margin Inflows and Controlling Development Outflow is Key to RoD

Source: Deloitte Consulting LLP

RoD is simple to visualize, but no single improvement lever will consistently send sales soaring. Focus is required on every aspect of the management and operational processes of product development, from critical attention to portfolio-level economics and the minute details of each engineer's work patterns. RoD can provide a valuable collecting point for tying together multiple improvement efforts, all sharing a common objective of making the NPV of gross margin from development substantially exceed the NPV of development cost to meet your profitability and growth objectives. ∎

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Mark Davis is a principal in Deloitte Consulting LLP's Silicon Valley office and leads the firm's product development practice. He has over 22 years of experience helping companies improve strategic and operational processes around product development and supply chain. You can reach Mark Davis at mardavis@deloitte.com or 408-464-6060.

John La Bouff is a 30-year veteran of the semiconductor industry, and was among the first to develop supply chain practices and systems designed around the fabless model. John is now a senior manager in Deloitte Consulting LLP's Silicon Valley practice, where he focuses on operational performance and product development improvement for semiconductor companies. You can reach John La Bouff at jlabouff@deloitte.com or 650-450-6056.

proceedings. One Tier 1 global electronics company said they knew they had a problem, and they even used a sophisticated brand protection solution to find the violators, but then they didn't do anything about it. They were not sure what steps to take. Their in-house legal council did not have experience in this area, and the whole process bogged down. Meanwhile, the executive who was focused on this problem reported that their company could save $20 million in one year if they'd only be organized enough in the enforcement area. He believed the counterfeiters knew they weren't going to do anything about the problem, and he said their company was actually helping keep the violators in business.

What enforcement steps can a semiconductor company take to ensure success? There are some very easy and cost-effective initial steps that can be taken. First, once a company determines a suspect selling counterfeit products, today's Software-as-a-Service (SaaS)-based brand protection/anti-counterfeiting solutions offer automated cease and desist (C&D) and Digital Millennium Copyright Act (DMCA) letters. Often, this is enough to let violators know that a manufacturer is watching them and will take enforcement steps. Many of these counterfeiters will then move onto other companies that are not so vigilant.

Of course, the most sophisticated violators require stronger enforcement procedures. Once a suspect is identified, a test buy is often required. Investigators experienced in test buys set up bogus companies and bank accounts so the suspect does not get suspicious. Some semiconductor companies with larger brand protection teams may want to do the test buys themselves, setting up their own fake company. After the product has been analyzed and certified

as a counterfeit, in addition to a C&D letter, there are a number of legal steps that can be taken without involving time-consuming and costly court battles. There are a number of legal firms that focus specifically on this area, can work closely with an in-house council and have honed to process so they get results in less than 90 days. The important point here is that once suspects know that a company is proceeding with enforcement, they will often stop. The more sophisticated counterfeiting syndicates will stay away from a semiconductor company with a reputation for stringent enforcement.

By gaining management support and committing some resources, whether it's a brand protection team, a brand protection solution with advanced online monitoring or taking some greater enforcement steps, semiconductor companies can stop helping counterfeit activity grow. And at the same time, they'll be saving their company millions or billions of dollars in lost revenue, brand reputation and customer satisfaction. ∎

About the Author

Chris Jensen is vice president at New Momentum, a SaaS-based anti-counterfeiting/brand protection solution that identifies counterfeit offenders who are offering goods for sale on the Internet. Using advanced search technology, New Momentum finds sales of electronics products in places that are out of reach through traditional methods. In addition to 24/7 monitoring, New Momentum's solution filters out the noise and prioritizes the violators in an intuitive user dashboard or reports. This prioritization of suspects makes it easy to determine who to start enforcement proceedings on first for greater ROI. New Momentum even provides automated C&D or DMCA letters, auction shutdowns and test buy services. You can reach Chris Jensen at cjensen@newmo.com.

parties all seeking advantage out of a common endeavor; therefore, success hinges on tailoring execution to each class of participant. This is the role of execution hubs.

Partner Hub

The partner hub manages standards of interaction between partners. Basically, it guides decisions on sharing—who collaborates and what is shared. And it drives decisions on data, rules, specifications and tools—which will be used, in what programs and by whom. The hub inserts logic for data, rule and specification by process step so that at execution time each member possesses the complete and correct elements for success. Additionally, it summons the common and shared tools when the team needs them to drive predictable and timely results.

Provider Hub

The IP providers form an integral part of the collaboration's success, and therefore the provider hub formalizes and manages their roles and the use of their IP. Providers can then reach a larger audience of users and serve them more efficiently than by working with multiple individual companies with disparate roles and methodologies. By the same token, the collaborators receive more robust service at a lower cost than they can individually.

Client Hub

The success of all programs ultimately depends on the ability of the product or service to satisfy the client. Since a consortium's efforts comprise a huge investment while representing a diverse body of client needs, it benefits members to facilitate a level of managed client participation. The primary client engagement drives requirements into specifications and specifications into the partner and provider hubs. The client hub provides clients with a level of review and requirement tracking that keeps the collaborators on course. Ultimately, however, the client hub can facilitate co-opted design by leveraging client insights into usable products.

Commerce Hub

How do collaborators manage the value of their assets used in common? This management complexity escalates as the number of collaborators with assets grows rapidly. An efficient way of handling this is to create a commerce hub as a marketplace for members to bid on the assets introduced. Since leading companies offer and need multiple assets, the execution process can provide a netting algorithm so that little cash, if any, changes hands. Concurrently, the hub maintains proprietary protection rules and usage control for all assets within its domain.

Figure 2. Execution Hubs
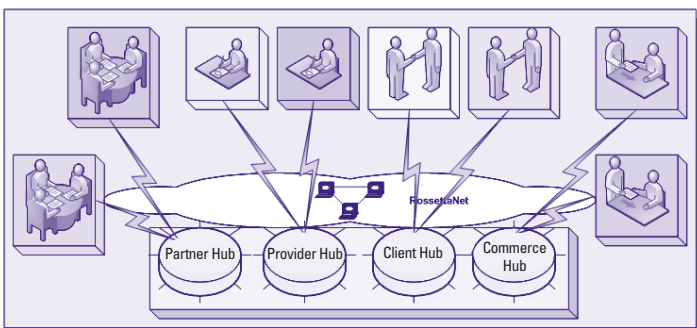
Execution Management – Common, Real-Time and Interactive Process

Execution hubs establish forums for mutual guidelines. Execution management creates common, real-time and interactive processes.

Preparation

Most programs fail in the beginning. A well-designed execution engine engages participants—partners, providers and clients—at the outset in a structured process of program concept and requirements definition. In parallel, the engine engages manufacturing teams to validate the program's manufacturability rules. Ensuring that the preparation is complete and correct, the engine allows the program to exit the gate to development.

Engagement

The execution engine drives linkages throughout the program as shown in Figure 3 by connecting participants, data, ground rules, specifications and tools at the correct point. Constructed in modular building blocks, the engine ensures connectivity and handoffs end to end, top to bottom to top, site to site and owner to owner. This structure provides the massive parallelism required for integrating clients with development, design and manufacturing teams.

Monitor, Assess and Control

As the program progresses, the engine disseminates process status for monitoring, assessment and control. This allows for rapid response to excessive process variances and aberrations, thereby maintaining continuity. Summarized, it enables continuous process improvement.

Figure 3. Execution Management
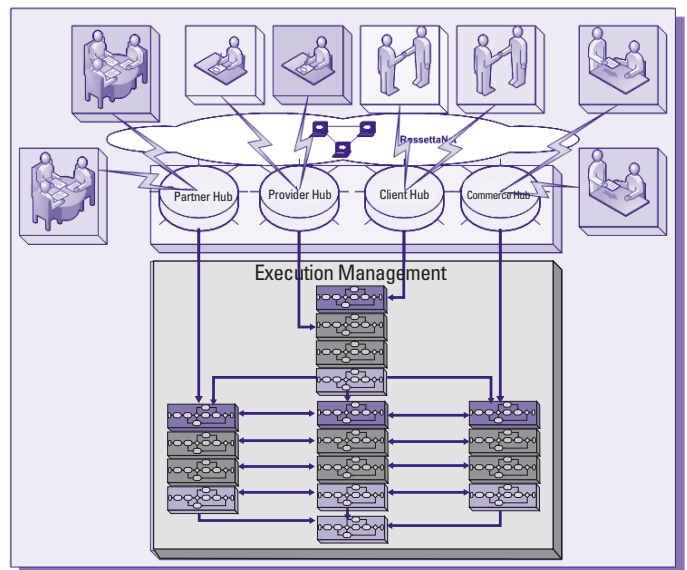
Summary

Aircraft industry programs suffered significant setbacks from problems of global partnerships:

- Lockheed Martin F35 JSF.
- Boeing 787.
- Airbus A380.

The semiconductor industry, with development costs reaching billions of dollars, cannot afford such disconnects. Many semiconductor operational executives recognize global collaboration

as a paramount requirement for their continued success. These leaders will take the initiative to transform their partnerships into true collaborative enterprises. ∎

About the Author
Mr. Enright established Enright Enterprise Consulting Solutions LLC in 2009 to provide globally collaborative enterprises with innovative strategies, methods, tools and architecture to enhance their competitiveness. Mr. Enright, an IBM Certified Consultant, spent eight years in IBM's Systems and Technology Group playing a leadership role in transforming manufacturing and the supply chain from an in house-only provider to a globally collaborative one. Mr. Enright also served in many leadership roles at Digital Equipment Corp for nearly twenty years. Mr. Enright holds an MBA degree from the University of Virginia's Darden School. You can reach Mr. Enright at kerry.enright@enrightenterprise.net or 951-816-9581.

experience and engineering practices, on how to get the most out of every die they manufacture.

So while I believe the wafer foundry is the most important member of the supply chain, if one cannot access their capability, it's all for naught. And that's the value-add of the VCP.

Q: *While outsourcing production operations and logistics services has proven to be a cost-effective strategy for fabless companies, it is still a relatively new concept. How will the eSilicon Investment Fund help convince wary CEOs to adopt this new business model? Looking forward, how do you project this approach will impact the industry in terms of growth and innovation?*

A: The purpose of the eSilicon Investment Fund is to bridge the financial gap that arises while transitioning activities (e.g., transferring inventory and ramping new products) from being managed in-house to being outsourced to eSilicon. This novel resource will help our customers get over any humps that may occur and move them gracefully to an outsourcing model, and we've been very successful with this to date.

Outsourcing production operations and logistics services to a VCP such as eSilicon improves top-line and bottom-line business performance. From a top-line perspective, with a VCP overseeing a company's operations, they have more time to focus on producing a greater number of chips, allowing them to have six product lines, instead of four. From a bottom-line perspective, the job of a VCP is to eliminate inefficiencies from the ecosystem by helping customers use wafers more successfully, choose the right IP and package, reduce test times by the efficient use of EDA tools and so on. We simply know that a VCP can purge billions of dollars out of the semiconductor industry, thereby putting more money in the pockets of the customers, suppliers and, of course, VCPs. This all translates into lower product prices and more successful products in the market.

Q: *The struggling EDA industry is attempting to transform itself through broadening its market to include IP and embedded software tools, as seen through the acquisitions of Virage Logic and Denali Software by Synopsys and Cadence Design Systems, respectively. What are your thoughts on the potential transformation of the EDA industry, and how will it impact eSilicon's business of providing integrated solutions?*

A: The EDA industry is obviously struggling, and it has to make some strategic moves to rebound. I believe that IP is a very legitimate place for them to add value and extend their reach. The IP industry's compensation is primarily based on royalties, which is a success-based model. If the EDA industry abandons the success-based model as they enter the IP space in favor of the upfront fee—in other words, increases prices at the elimination of the royalty payable on successful units shipped—it will start to look more and more like the current compensation scheme for EDA tools. This approach will just drive them further into a hole, which is how they got there in the first place.

From an eSilicon perspective, we like the aggregation of IP into fewer, larger and more competent companies. This gives companies the economies of scale that allows them to depend on the quality and the durability of their IP. However, the pricing model will determine whether or not it is perceived as positive or negative in the long term.

Q: *Tell us about eSilicon's recent partnership with design services and IP firm S3 Group and how customers will benefit more from this partnership than relying on traditional design services providers.*

A: S3 Group is an outstanding design, IP and information technology (IT) company, and they specialize in a development area that eSilicon does not. The company develops specification-level designs, does some physical design work and supplies quality IP. As I mentioned earlier, eSilicon generates revenue by shipping silicon, so this is a natural partnership where S3 Group provides design services and we provide manufacturing and productization services. As the industry moves into greater complexity, mutual understanding between design and manufacturing is critical in getting a chip to market on time and making sure it performs well. This partnership will enable that to happen.

Q: *According to iSuppli, the industry is currently maintaining lean inventory levels, which is extending lead times and resulting in commodity component shortages. Do you see lean inventory levels right now? How can eSilicon help companies improve supply chain visibility, inventory management and properly forecast product demand? What is a healthy inventory level?*

A: Yes, inventory levels are low today, and there is legitimate demand for products. None of our customers are building inventory, and I've heard that many of the largest suppliers in the supply chain are forbidding their customers to build inventory. If a supplier gets any wind that the chip company's sell through demand is not equal to what they are buying, they are being cut off because there's such a scramble for scarce resources right now.

In exchange for the chip company's 12-month rolling forecast, eSilicon provides the customer with pricing up to three to four years in advance, whereby we take the risk of cost in the marketplace. This is something that no other supplier in the industry does. When we supply forecasts to our supply chain, they know that it is for a much longer period than what they would typically get themselves; that we take forecasts very seriously because it is how we make our money; and that we pay close attention to the actual success of our customers since we've committed to give them future pricing. This discipline also translates into better inventory management. If we communicate to our suppliers that we know what the demand will be and they commit to that delivery, then our customers know they can count on a consistent supply of product and thereby have less of a requirement to build inventory.

A healthy inventory level varies among industry sectors. For example, a healthy chip inventory level for a cell phone business is higher than for a network processor chip business. ∎

materials and distribution strategies to minimize waste, energy use and emissions from transportation.

Figure 3. DfE Concepts
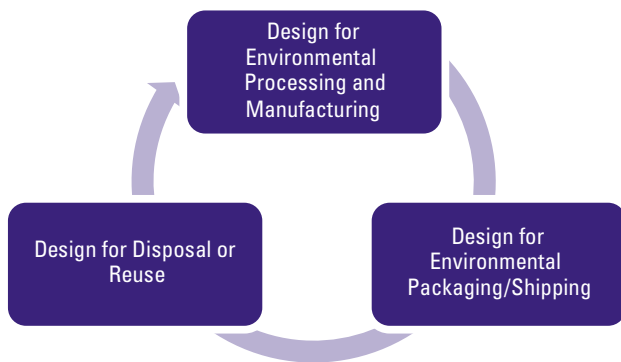
Green Supply Chain Management

The idea of green supply chain management (GSCM) is to eliminate hazardous materials and minimize waste (energy, emissions, landfill material, etc.) during procurement, manufacturing, distribution and reverse logistics. It is important to identify and qualify suppliers who follow RoHS directives, are ISO14000 and OHSAS18000 certified, and have a CSR program or adhere to commonly accepted codes of conduct such as those from EICC. Generating and maintaining an approved suppliers list will help ensure that only suppliers capable of providing compliant materials or components will be used. The suppliers' environmental performance should be assessed periodically through audits to ensure ongoing compliance. It is also useful to establish partnerships with strategic suppliers to share roadmaps and generate action plans that will lead to continuous improvement in environmental compliance for both parties.

Collecting, Managing and Disseminating Compliance Data

Most electronic products are too complex, and the supply chain is too dynamic today to rely on manual documentation methods. Documenting product compliance electronically in a database system is essential. Some companies have customized their product lifecycle management or enterprise planning systems to address product compliance, while others have chosen to use third-party software tools. When customizing or looking for new software tools, it is important to address data importing, error checking and ability to produce customer- or regulation-specific reports to avoid resource-intensive manual generation.

Obtaining compliance data from component suppliers and subcontractors is becoming less challenging than it used to be since mainstream suppliers are now starting to post the data on their Web sites. In many cases, however, the data must still be requested through a sales or technical support portal which may take significant time and effort. This issue should be taken into consideration when selecting suppliers.

The most widely accepted standard reporting format for electronic data exchange of environmental data is the IPC-1752x Material Declaration family. Unfortunately, use of the IPC standard is not universal, so data may come in a variety of formats. Standardize reporting formats for electronic data exchange with suppliers whenever possible, so importing data can be done quickly and at the lowest cost. When standardization is not possible, special software

utilities can sometimes be used that can handle uploading of different data formats into an environmental compliance database to avoid tedious and error-prone manual entry. Gathering compliance data from a variety of sources and building a technical compliance file can significantly reduce the risk of making incorrect representations about a product (Figure 4). Components of a typical product technical compliance file:

- Homogenous material composition data.
- Material safety data sheet (MSDS) for homogeneous materials.
- Third-party analytical test data for materials.
- Supplier declarations of conformity.
- Supplier audits.
- Relevant technical publications available on the Internet.

Figure 4. Risk vs. Resources
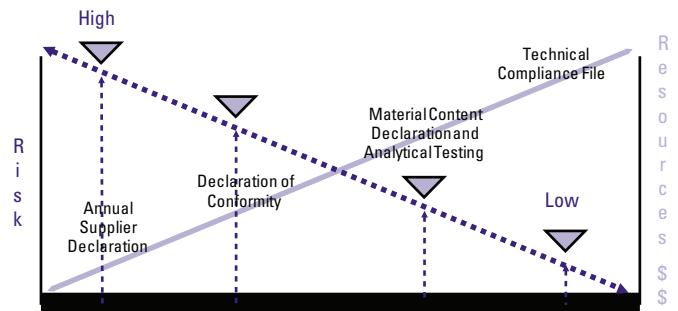
Conclusion

Companies that take a systematic approach to environmental compliance can develop a sustainable system that provides maximum product compliance at the lowest cost. Develop a proactive approach to stay on top of new and changing regulations, and make sure compliance is consciously built into the product during the early specification and design stages. Partner with suppliers who are serious about reducing their environmental impact since they will most likely have continuous improvement programs which will lower the risk of getting non-compliant materials. Standardize and automate as much of the technical compliance data management process as possible to reduce resources, costs and errors. Strive for higher levels of disclosure now, which will minimize additional work needed later as more stringent regulations come into force. Companies that embrace ongoing environmental compliance practices now will be more competitive in the global market moving forward. ∎

About the Authors

Tom Krawczyk is the compliance manager at Conexant Systems Inc. He is responsible for RoHS/environmental and ISO compliance for the company. Tom has 18 years experience in the semiconductor industry, and has spent the last six years following the development of worldwide environmental regulations while developing and improving systems utilized at Conexant to meet worldwide compliance obligations. You can reach Tom Krawczyk at tom.krawczyk@conexant.com.

Robert Warren is director of packaging engineering and supplier quality at Conexant Systems Inc. He has over 20 years of experience in the semiconductor industry, holds over a dozen patents, has published numerous technical articles and is co-author of an advanced electronics packaging textbook. He holds a B.S. in chemistry from University of Arizona and an MBA from University of Redlands. You can reach Robert Warren at robert.warren@conexant.com.

Figure 2. DSI System Diagram
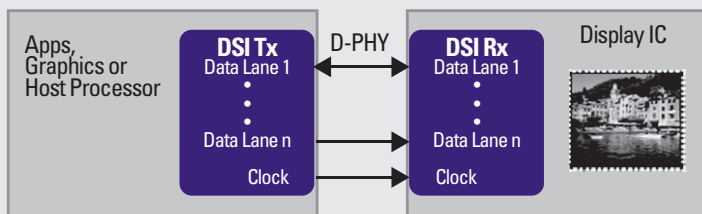
DSI is a HS, high-resolution serial interconnect bus offering connectivity to video display devices. DSI uses MIPI standard D-PHY for physical layer uni- and bi-directional HS differential interfaces with up to four data lanes and a common differential clock lane. Pixel data and commands are serialized into a single physical stream, and status can be read back from the display.

The protocol supports host and device technologies needed in the application processor, display panel and bridging applications. It also supports display devices operating in video mode and command mode.

Figure 3. CSI-2 System Diagram
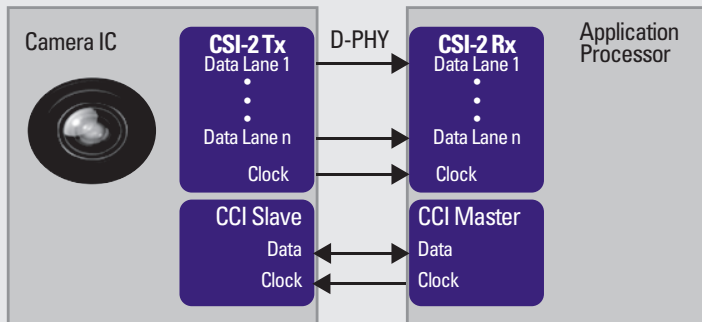
CSI-2 is a high-performance serial interconnect bus for mobile applications connecting camera sensors to digital imaging modules such as a host processor or image processor. CSI-2 uses MIPI D-PHY for physical layer and unidirectional HS differential interfaces with up to four data lanes and a common differential clock lane. A separate control channel interface (CCI) is used for interfacing and controlling signals between the host and camera. It supports host and device technologies needed in the application processor, camera sensor and bridging applications.

All these off-the-shelf standard interfaces enable LP, low pin count and low EMI-scalable interfaces with high-bandwidth capability.

MIPI Protocols in Action

A teardown of an LG KM900 cellular phone shows adoption of MIPI technology. An AMD Imageon A250 application processor employing a CSI Rx controller and D-PHY interacts with a 5-MP camera. This scalable architecture can easily change the 5-MP camera IC to an 8-MP camera IC, hence introducing a higher tier version of the phone in a new model quickly and cost effectively.

The MIPI CSI also allows for the overall reduction of power, EMI emission and number of pins which can reduce costs and increase reliability and value to the end user.

Figure 4. LG KM900 Cellular Phone Teardown
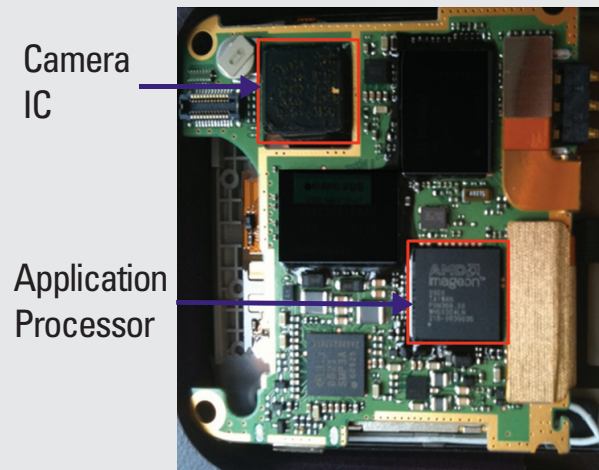
Meeting the Needs of Mobile Semiconductors

Balancing the requirements for faster, lower power and lower cost devices is part of the formula to achieving success. Managing systems and resource allocation based on tasks that provide differentiation, versus standard tasks that can be outsourced or acquired, is another part. Partnering with a trusted IP provider enables rapid market penetration and helps ensure the first silicon works to specifications.

Since cameras and displays have an asymmetric bandwidth requirement, application-optimized implementation can benefit the semiconductor vendor with dramatically reduced area and power. Furthermore, since these designs are typically fabricated at advanced process nodes, production yield and ramp plays a significant role. Adding calibration circuitry to the D-PHY implementation can reduce the risk of process variation and allows for improved signal integrity and yield loss recovery.

Mobile electronics market growth will be fueled by the wide adoption of MIPI specifications which will eliminate incompatibilities and fragmentation in interfaces, increase system reliability and quality, improve productivity by focusing energy on value-added differentiation, and facilitate innovation. Improving the ability of electronics manufacturers to respond to end-user needs effectively and rapidly will help increase satisfaction, thus increasing the usage of mobile electronics. ∎

About the Author

Hezi Saar serves as senior product marketing manager at Virage Logic and is responsible for its SiPro advanced interface IP product line which includes MIPI, High-Definition Multimedia Interface (HDMI), DisplayPort and Peripheral Component Interconnect Express (PCI Express). He joined Virage Logic in 2009, bringing more than 15 years of experience in the semiconductor and electronics industries in embedded systems and marketing positions to the company. Prior to joining Virage Logic, from 2004 to 2009, Hezi served as senior product marketing manager leading Actel's Flash field-programmable gate array (FPGA) product lines. Prior to that, Hezi served as a product marketing manager at ISD/Winbond and as a senior design engineer at RAD Data Communications. Hezi holds a Bachelor of Science from Tel Aviv University in computer science and economics and an MBA from CSU.

References
[1]*wikipedia.org, June 2010.*

test the integration of hardware with software. In fact, increases in design complexity and the explosion of embedded software require processing of billions of verification cycles in a short amount of time. Logic simulation is not up to the task because of its intrinsically slow execution time, and ESL simulation, albeit fast in execution, does not offer the hardware design accuracy to trace hardware bugs.

This is where emulation can help. At a speed of 10 MHz, the latest generation of emulation platforms can execute one-billion cycles on a 10-million gate design in a little more than one minute. They can provide full access to the entire design for quickly locating defects, whether in hardware or in software, and reduce re-spins and accelerate embedded software development.

As many design teams will attest, fast emulation has become a critically important verification component for large and complex systems-on-chip (SOCs). Today, emulation is used to test the hardware aspects of a SOC design and to verify the integration of hardware and the embedded software. It is possible to start RTL verification at the block level and move on to the system level as the entire design takes shape. Emulation can also co-verify the interaction of hardware and software once the full RTL design is complete.

This alone could justify an emulator's ROI. Hardware and software designers are able to share the same system and design representations due to combined software and hardware views of the design. With this information, they are able to work together to debug hardware and software interactions. They can track a design problem across the boundary between the embedded software and the hardware to find the problem.

Emulation's traditional use as a means for in-circuit testing has been expanded to where they now support complex test environments, including hardware description language (HDL) testbenches; transactional C++, SystemC or SystemVerilog testbenches or test models; and test vectors. Hard cores, such as those provided by ARM, MIPS and others, can be accommodated through a dedicated module as well.

And that's not all. Newer generations of emulation platforms have gone green with cutting-edge technology. These platforms consume far less power than their earlier, big-box counterparts because the power dissipation of a big-box emulator wastes energy to cool the rooms where they reside, resulting in a lower monthly energy bill. It also means maximizing energy efficiency and decreasing a company's carbon footprint, easing up on the power grid. The range of power consumed per box is about 1 kW for a 100-million ASIC gate green emulator. A big-box emulator with equivalent capacity consumes more than 10 kW.

Newer emulation machines have smaller footprints, physical dimensions and weight, and have fewer parts and components than big-box emulators.

The dimensions of a big-box emulator with a capacity of 100-million ASIC gates exceed 50x30x40 inches, while the size of a green emulator with equivalent capacity is less than 20x20x10 inches. The volume of 33 cubic feet for the big box compares to a volume of about two cubic feet of the green emulator. As far as the weight of each, big boxes weigh somewhere around 1,000 pounds, while smaller emulators weigh only 70 pounds for an equivalent configuration.

When multiple boxes are interconnected to increase overall design capacity, a 500-million gate design would require four large boxes—or 120 cubic feet of volume, about two tons of weight, more than 30 kW of power and adequate air cooling. An equivalent green emulator would occupy less than 15 cubic feet of space and weigh about 200 pounds, draining 5 kW of electricity with less air cooling requirements.

One obstacle to the widespread use of emulation has traditionally been the high purchasing price. Big-box emulators of the past were priced at tens of cents per ASIC-equivalent gate, preventing their deployment in volume and pervasive adoption.

Current pricing for an emulation platform varies, depending on capacity, speed and environmental requirements. Some more cost-effective emulators are priced at pennies per gate, while others start at about $1 per gate. All in all, this pricing makes them a great choice for a broad range of designs, regardless of complexities or topologies.

Overall, hardware emulation is a viable verification tool that can help design teams bring their chips to market on time and within budget, producing a solid ROI for any development project. While it's important to maximize the budget spent on capital expenditures, reaching high-volume shipments in time is even more critical to a company's long-term success. Using the right design flow, methodology and hardware emulation platforms will provide benefits across the product's entire development and improve ROI.

The EDA industry continues to be the foundation for the semiconductor industry. Those companies who can demonstrate that their products offer good value and a clear ROI should survive and emerge as the next-generation leaders of the EDA industry. The emulation sector, in particular, should produce a new set of leaders in the not-so-distant future. ∎

About the Author
Lauro Rizzatti is general manager of EVE-USA. He has more than 30 years of experience in EDA and automated test engineering (ATE), where he held responsibilities in top management, product marketing, technical marketing and engineering. You can reach Lauro Rizzatti at lauro@eve-team.com.

administrator, with the right support and tools, can be the project manager, negotiator, diplomat, programmer and in-house YMS expert that he or she needs to be to ensure the integrity of the yield data. A high level of data integrity of one's YMS database, in turn, encourages users to trust the data in the YMS database. ∎

About the Author
Nancy K. Tsai consults on yield management issues for semiconductor suppliers. She has over 10 years of experience working with both integrated device manufacturers (IDMs) and global semiconductor suppliers on a variety of yield data management platforms. She holds a Ph.D. in mechanical engineering from Stanford University. You can reach Nancy K. Tsai at nancytsai2000@yahoo.com.

References
[1] *As the saying goes, "Garbage In, Garbage Out."*

[2] *For example, can header formats be standardized for different products processed through the same tester platform at the same test supplier?*

[3] *Such a script could also check for duplicative downloads that waste bandwidth and degrade performance.*

[4] *Setting up a separate folder for each data type at each test supplier is one good practice.*

[5] *The extent of vulnerability depends not only on the potential for operator error in isolation but also on how given errors interact with the YMS. For example, data in a format not recognized by a parser could cause an entire datalog to be rejected.*